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MS-7B23

ATX:243.8mm*243.8mm

Ver: 2.2

Intel -CoffeeLake-S plamform

CPU:

LGA1151

*CPU POWER PAK *4Phase*

*GT POWER PAK *2 Phase*

Onboard Chip:

SIO: NCT5567D colay NCT5565D
HD Audio Codec: ALC887
LAN: RTL8111H
Flash ROM: SPI 64 MB

DP to VGA: RTD2167

CUT VBAT:SLG4B41231

Main Memory:

*DDR4 * 4 (Dual Channel)*

ACPI:

5VDAUL:uP7501

5VDIMM:uP7501

3VSB:GS7133+N MOS

1P8_VSB:GS7133

3VDSW:GS7116

VCCSTPLL:GS7133

System Chipset:

Cannon Lake B360

PWM:

VCORE - RT3606

DDR - RT8125E

DDR VPP25- MP2147

PCH(1.05V) - RT8125E

VCCSA - RT8125E

VCCIO - SY8288

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 2*

*M.2 Slot * 2*

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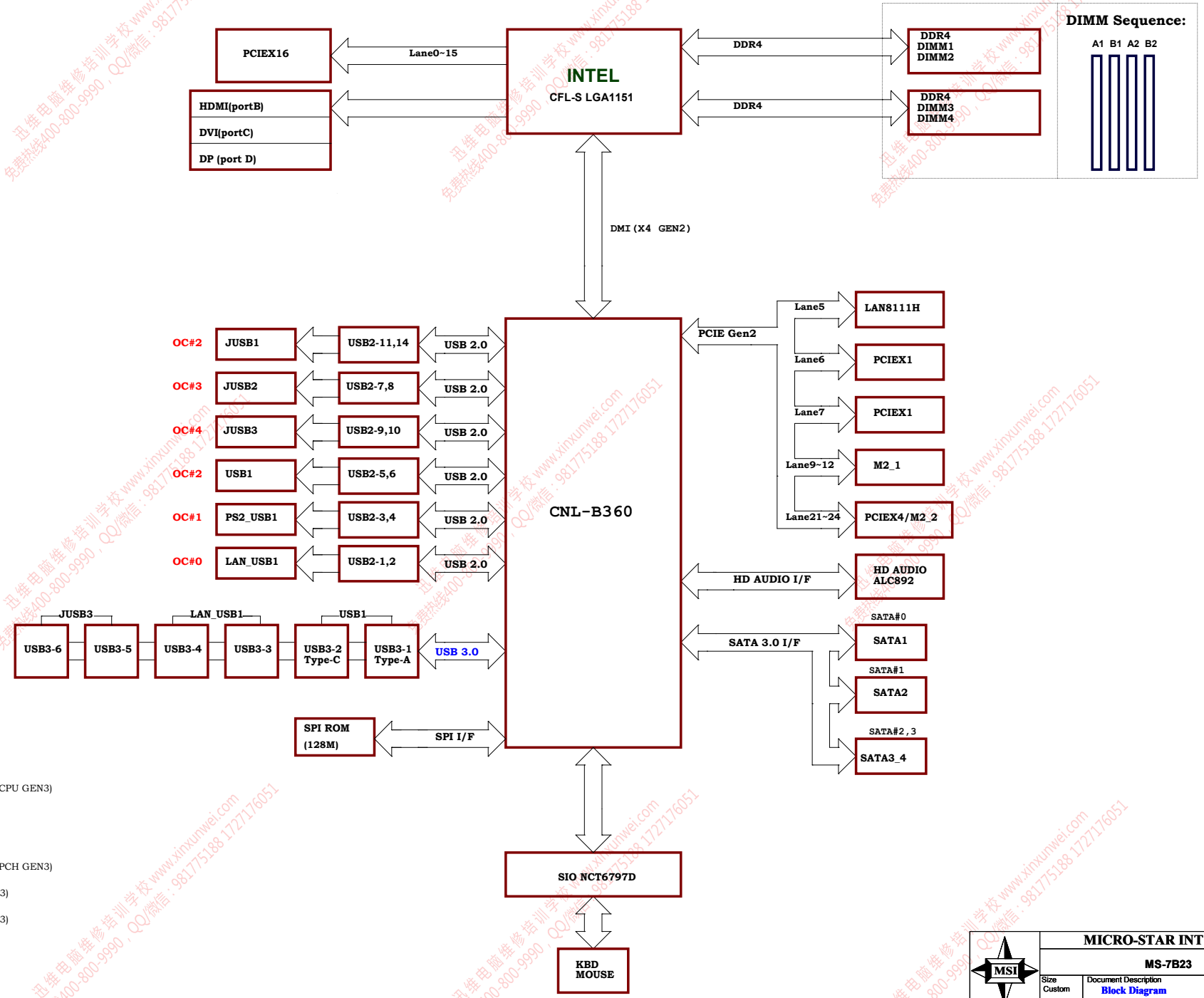
MS-7B23 Block Diagram



Slot Sequence:

PCIE X16	(By CPU GEN3)
PCIE X1	(By PCH GEN3)
PCIE X1	(By PCH GEN3)
PCIE X4	(By PCH GEN3)
M2_1	(By PCH GEN3)
M2_2	(By PCH GEN3)

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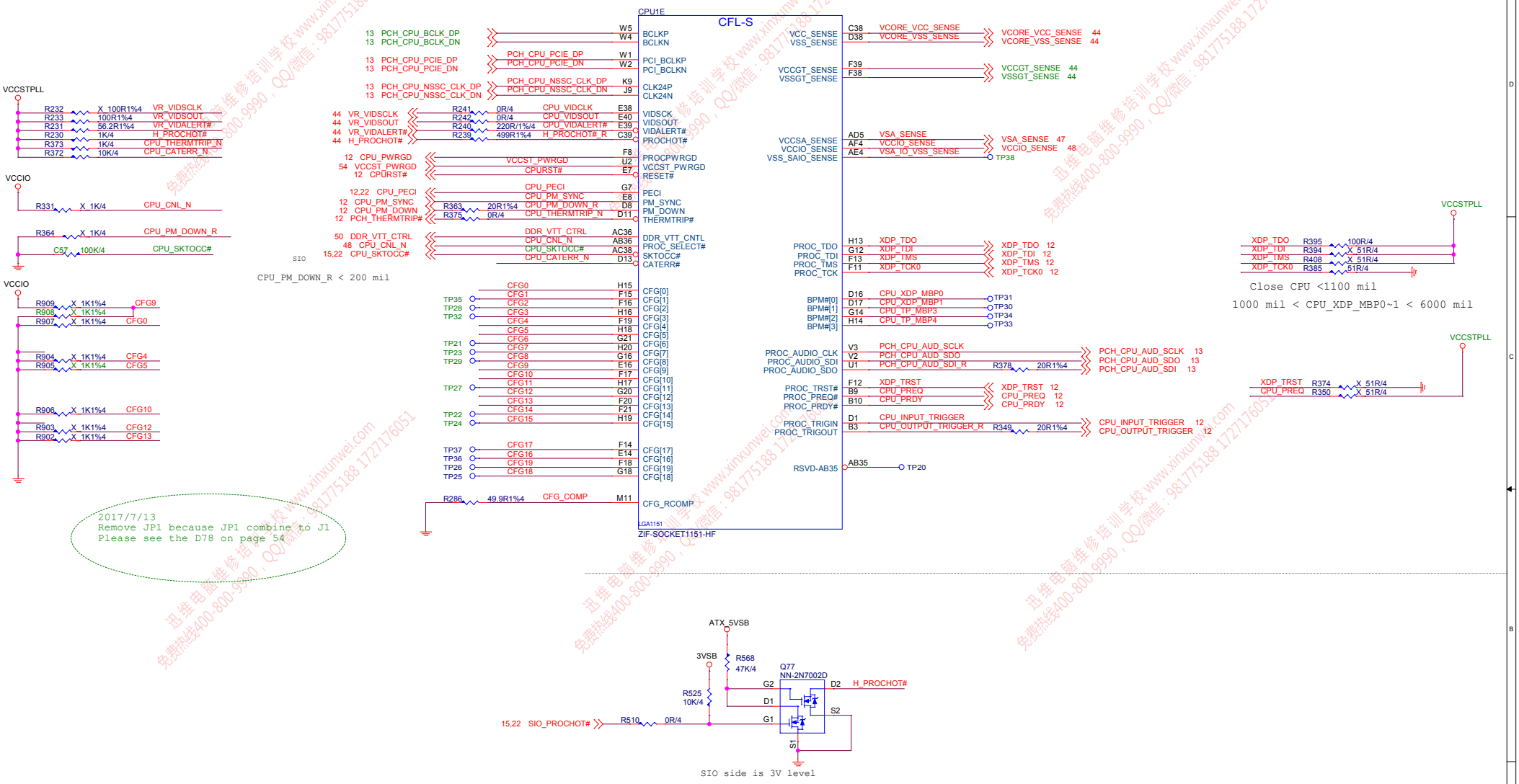

CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

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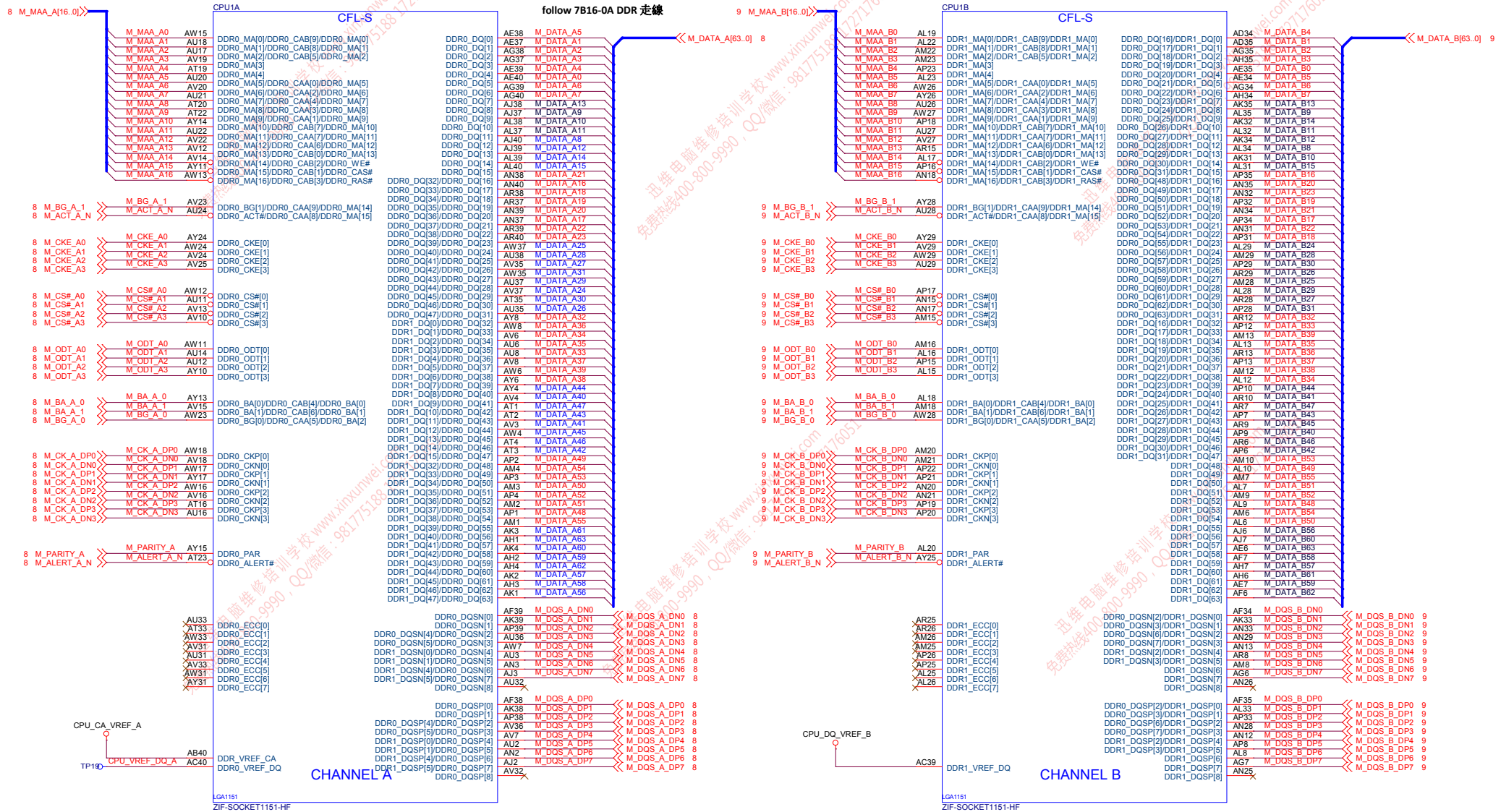
SOCKET PN N12-151A010-L06

follow 7B16-0A DDR 走線



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MS-7B23

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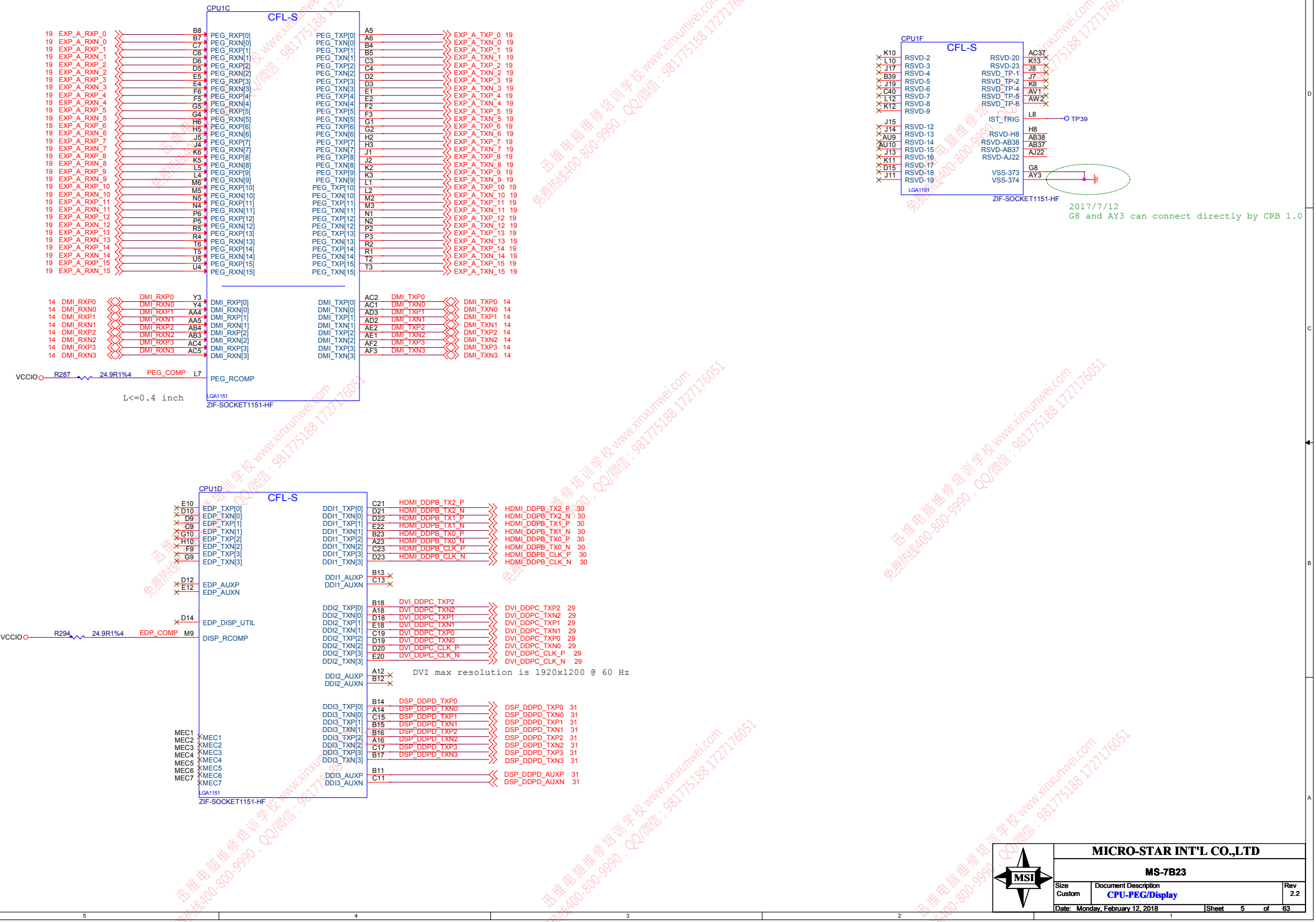
CPU1C
CFL-S
PEG_RXP[0..15]
PEG_RXN[0..15]
PEG_TXP[0..15]
PEG_TXN[0..15]
EXP_A_RXP_0 19
EXP_A_RXN_0 19
EXP_A_TXP_0 19
EXP_A_TXN_0 19
DMI_RXP0
DMI_RXN0
DMI_RXP1
DMI_RXN1
DMI_RXP2
DMI_RXN2
DMI_RXP3
DMI_RXN3
DMI_TXP0
DMI_TXN0
DMI_TXP1
DMI_TXN1
DMI_TXP2
DMI_TXN2
DMI_TXP3
DMI_TXN3
VCCIO
R287
24.9R1%4
PEG_COMP
L7
PEG_RCOMP
L<=0.4 inch
LGA1151
ZIF-SOCKET1151-HF
CPU1F
CFL-S
RSVD-2
RSVD-3
RSVD-4
RSVD-5
RSVD-6
RSVD-7
RSVD-8
RSVD-9
RSVD-12
RSVD-13
RSVD-14
RSVD-15
RSVD-16
RSVD-17
RSVD-18
RSVD-19
RSVD-20
RSVD-23
RSVD_TP-1
RSVD_TP-2
RSVD_TP-4
RSVD_TP-5
RSVD_TP-6
IST_TRIG
RSVD-H8
RSVD-AB38
RSVD-AB37
RSVD-AJ22
VSS-373
VSS-374
TP39
LGA1151
ZIF-SOCKET1151-HF
2017/7/12
G8 and AY3 can connect directly by CRB 1.0
CPU1D
CFL-S
EDP_TXP[0..3]
EDP_TXN[0..3]
EDP_AUXP
EDP_AUXN
EDP_DISP_UTIL
R294
24.9R1%4
EDP_COMP
M9
DISP_RCOMP
DDI1_TXP[0..3]
DDI1_TXN[0..3]
DDI1_AUXP
DDI1_AUXN
HDMI_DDPB_TX2_P
HDMI_DDPB_TX2_N
HDMI_DDPB_TX1_P
HDMI_DDPB_TX1_N
HDMI_DDPB_TX0_P
HDMI_DDPB_TX0_N
HDMI_DDPB_CLK_P
HDMI_DDPB_CLK_N
DDI2_TXP[0..3]
DDI2_TXN[0..3]
DDI2_AUXP
DDI2_AUXN
DVI_DDPC_TXP2
DVI_DDPC_TXN2
DVI_DDPC_TXP1
DVI_DDPC_TXN1
DVI_DDPC_TXP0
DVI_DDPC_TXN0
DVI_DDPC_CLK_P
DVI_DDPC_CLK_N
DVI max resolution is 1920x1200 @ 60 Hz
DDI3_TXP[0..3]
DDI3_TXN[0..3]
DDI3_AUXP
DDI3_AUXN
DSP_DDPD_TXP0
DSP_DDPD_TXN0
DSP_DDPD_TXP1
DSP_DDPD_TXN1
DSP_DDPD_TXP2
DSP_DDPD_TXN2
DSP_DDPD_TXP3
DSP_DDPD_TXN3
DSP_DDPD_AUXP
DSP_DDPD_AUXN
MEC1
MEC2
MEC3
MEC4
MEC5
MEC6
MEC7
LGA1151
ZIF-SOCKET1151-HF
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MS-7B23
Size
Custom
Document Description
CPU-PEG/Display
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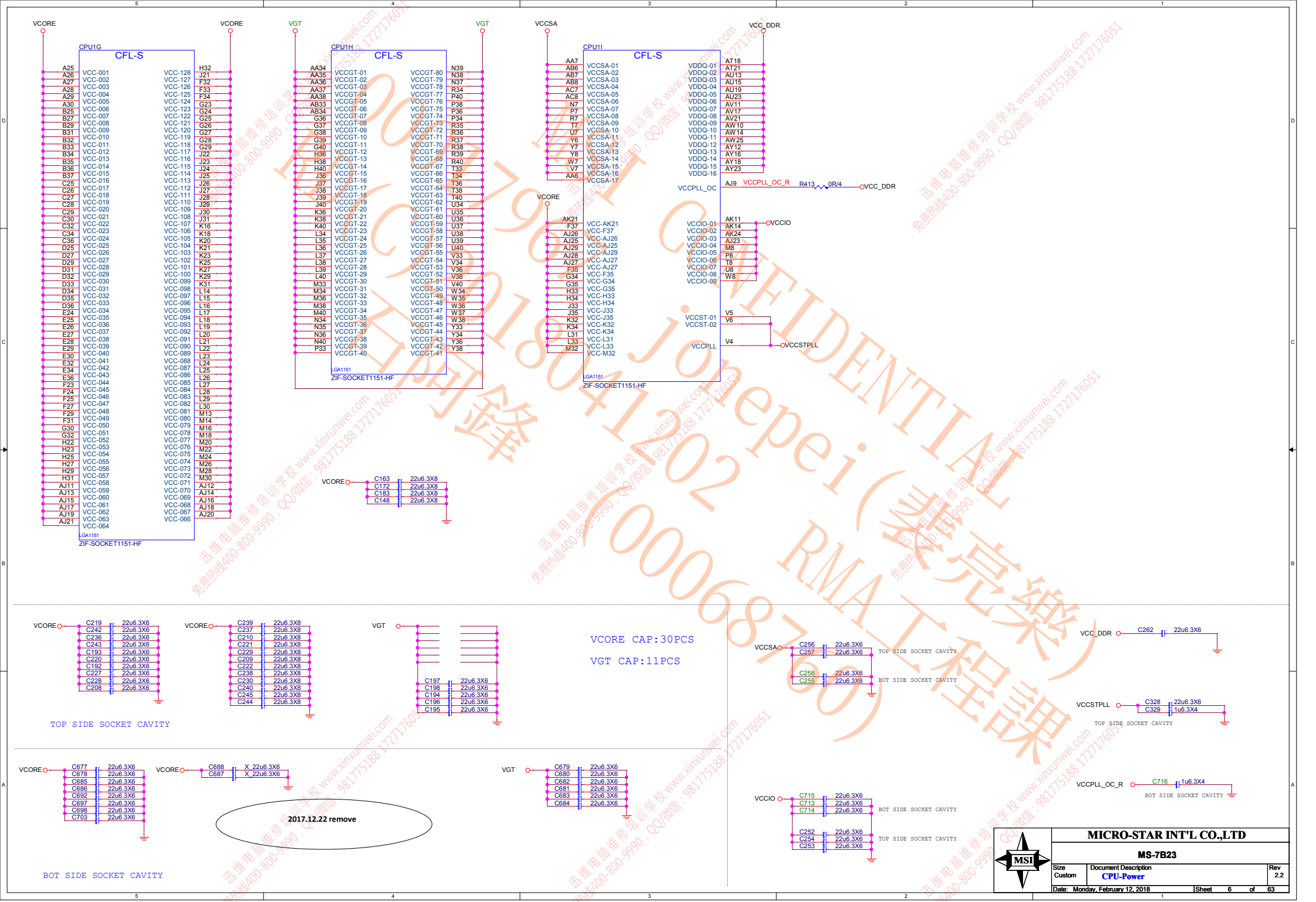

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(000687765)
2018/4/2
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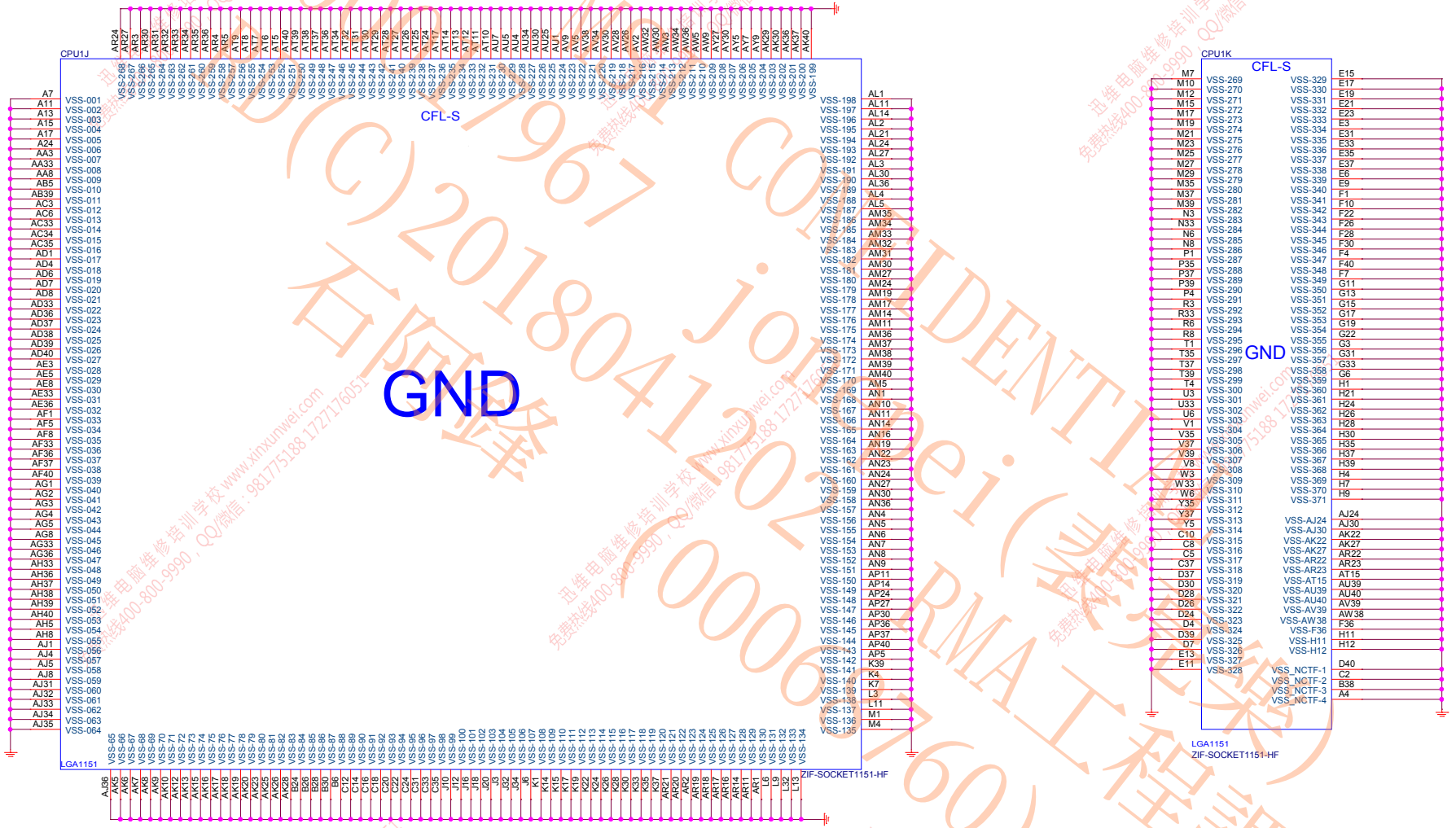

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Size: Custom	Document Description: CPU-GND		Rev: 2.2
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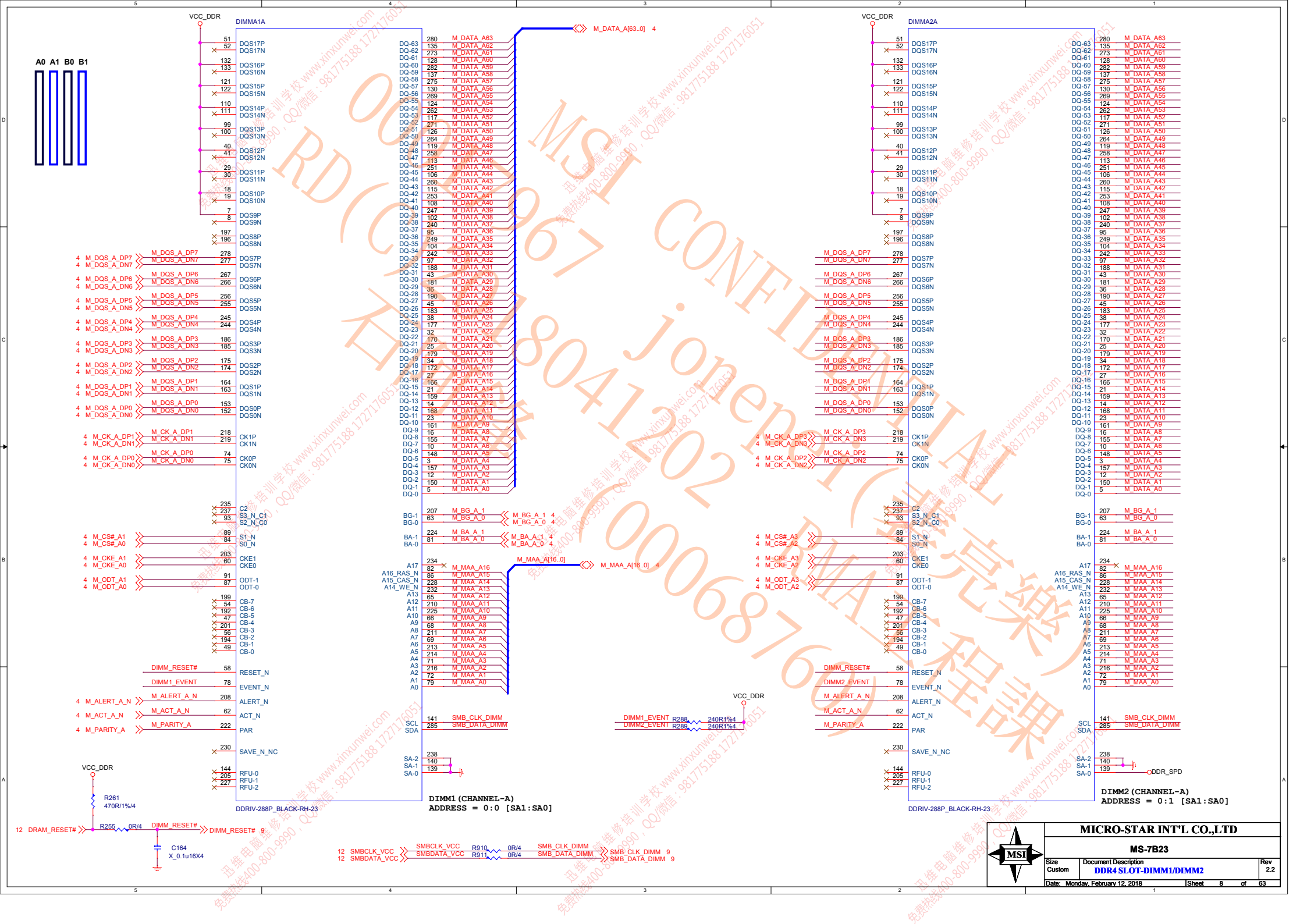
A0 A1 B0 B1
VCC_DDR
DIMMA1A
DDRIV-288P_BLACK-RH-23
DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
VCC_DDR
DIMMA2A
DDRIV-288P_BLACK-RH-23
DIMM2 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]
M_DATA_A[63..0] 4
M_MAA_A[16..0] 4
R261 470R/1%/4
R255 0R/4
C164 X_0.1u16X4
R910 0R/4
R911 0R/4
R288 240R1%4
R289 240R1%4
DDR_SPD
MICRO-STAR INT'L CO.,LTD
MS-7B23
Size Custom
Document Description DDR4 SLOT-DIMM1/DIMM2
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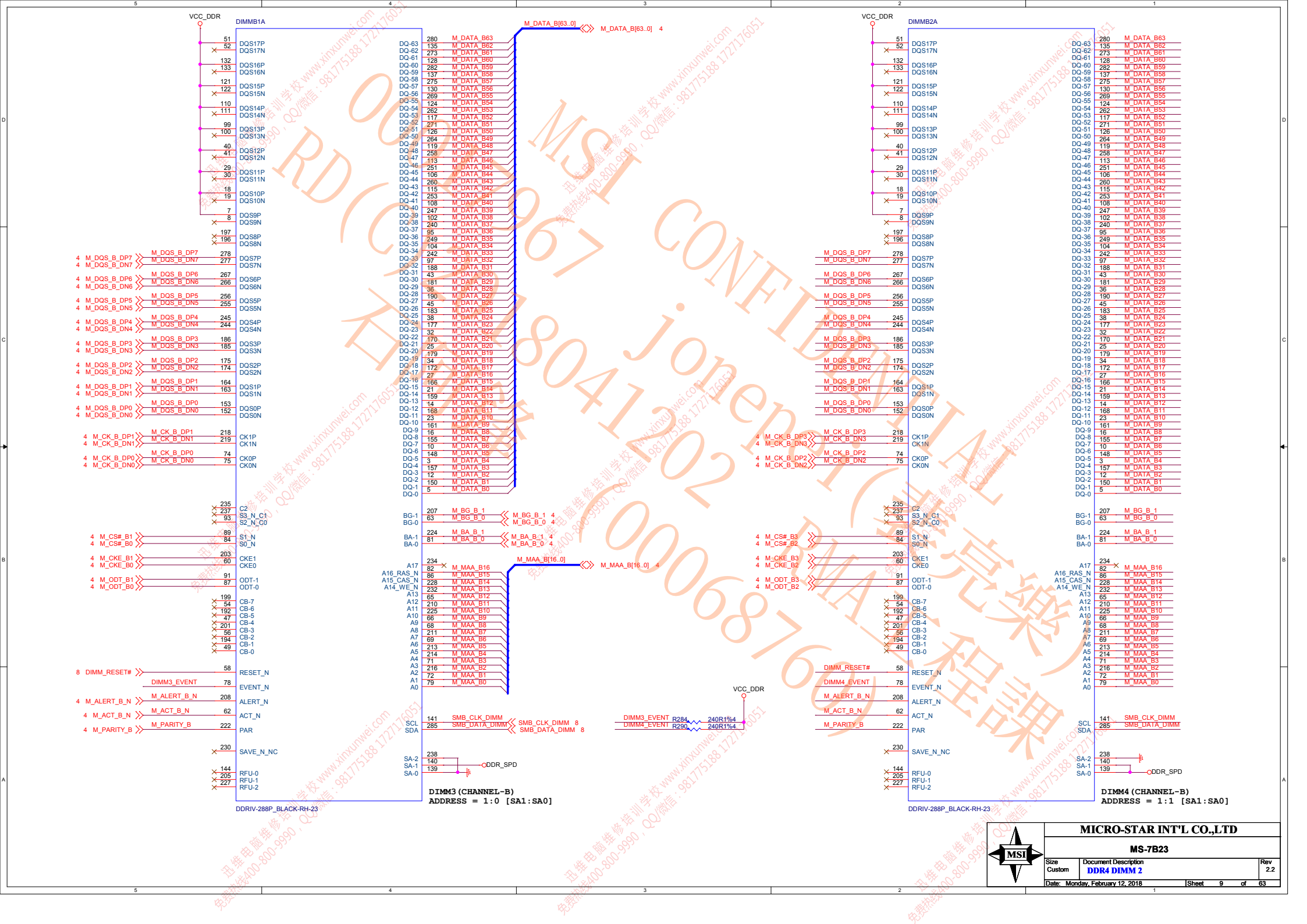
VCC_DDR
DIMMB1A
DDRIV-288P_BLACK-RH-23
DIMM3 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]
VCC_DDR
DIMMB2A
DDRIV-288P_BLACK-RH-23
DIMM4 (CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]
MICRO-STAR INT'L CO.,LTD
MS-7B23
Size
Custom
Document Description
DDR4 DIMM 2
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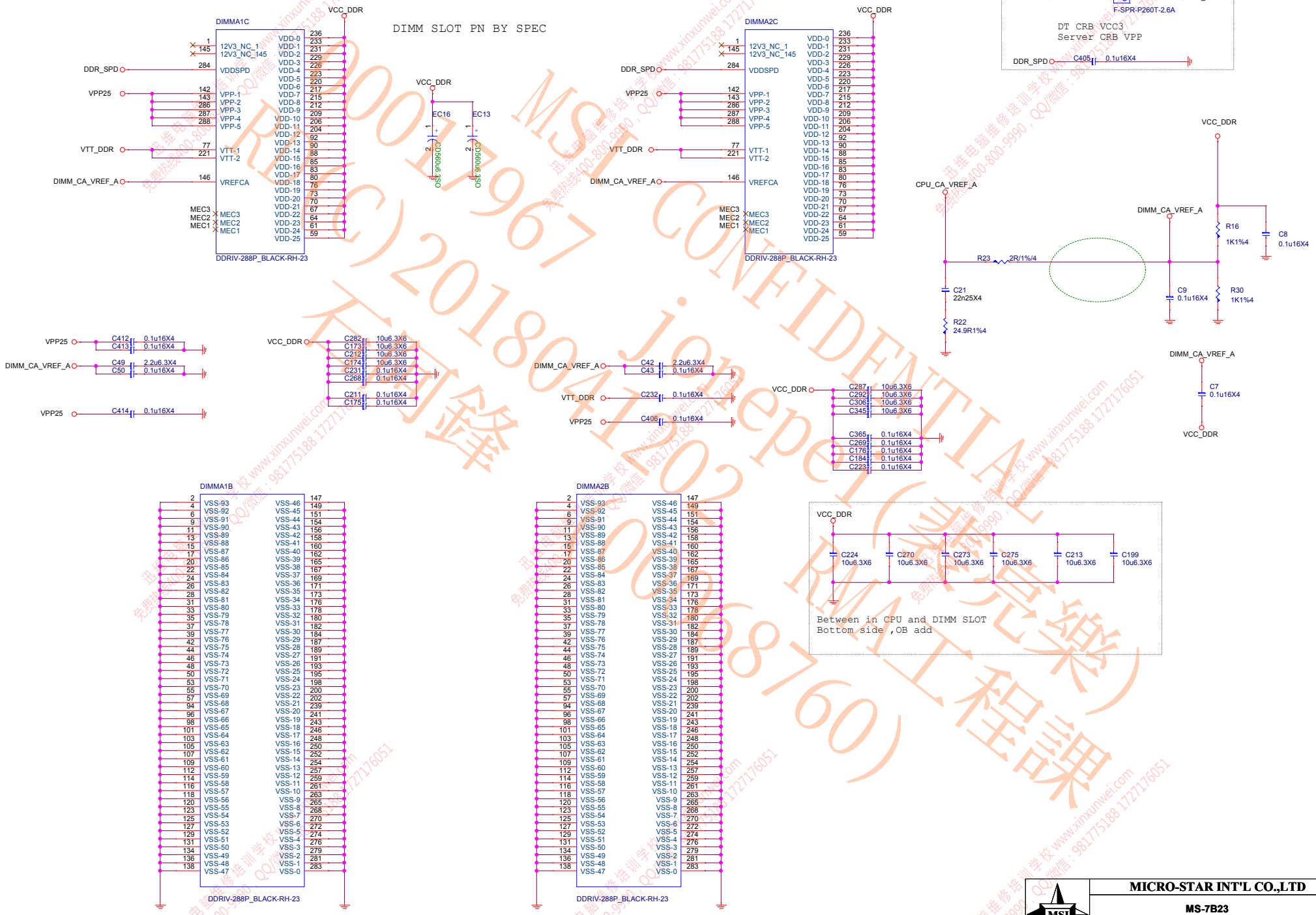
DIMM SLOT PN BY SPEC
DIMMA1C
DIMMA2C
DIMMA1B
DIMMA2B
DDRIV-288P_BLACK-RH-23
VCC_DDR
DDR_SPD
VPP25
VTT_DDR
DIMM_CA_VREF_A
CPU_CA_VREF_A
F4
F-SPR-P260T-2.6A
DDR_SPD
DT CRB VCC3
Server CRB VPP
C405 0.1u16X4
R23 2R/1%/4
C21 22n25X4
R22 24.9R1%4
R16 1K1%4
C8 0.1u16X4
C9 0.1u16X4
R30 1K1%4
C7 0.1u16X4
Between in CPU and DIMM SLOT
Bottom side ,OB add
MICRO-STAR INT'L CO.,LTD
MS-7B23
Size Custom
Document Description
DDR4-POWER/GND-1
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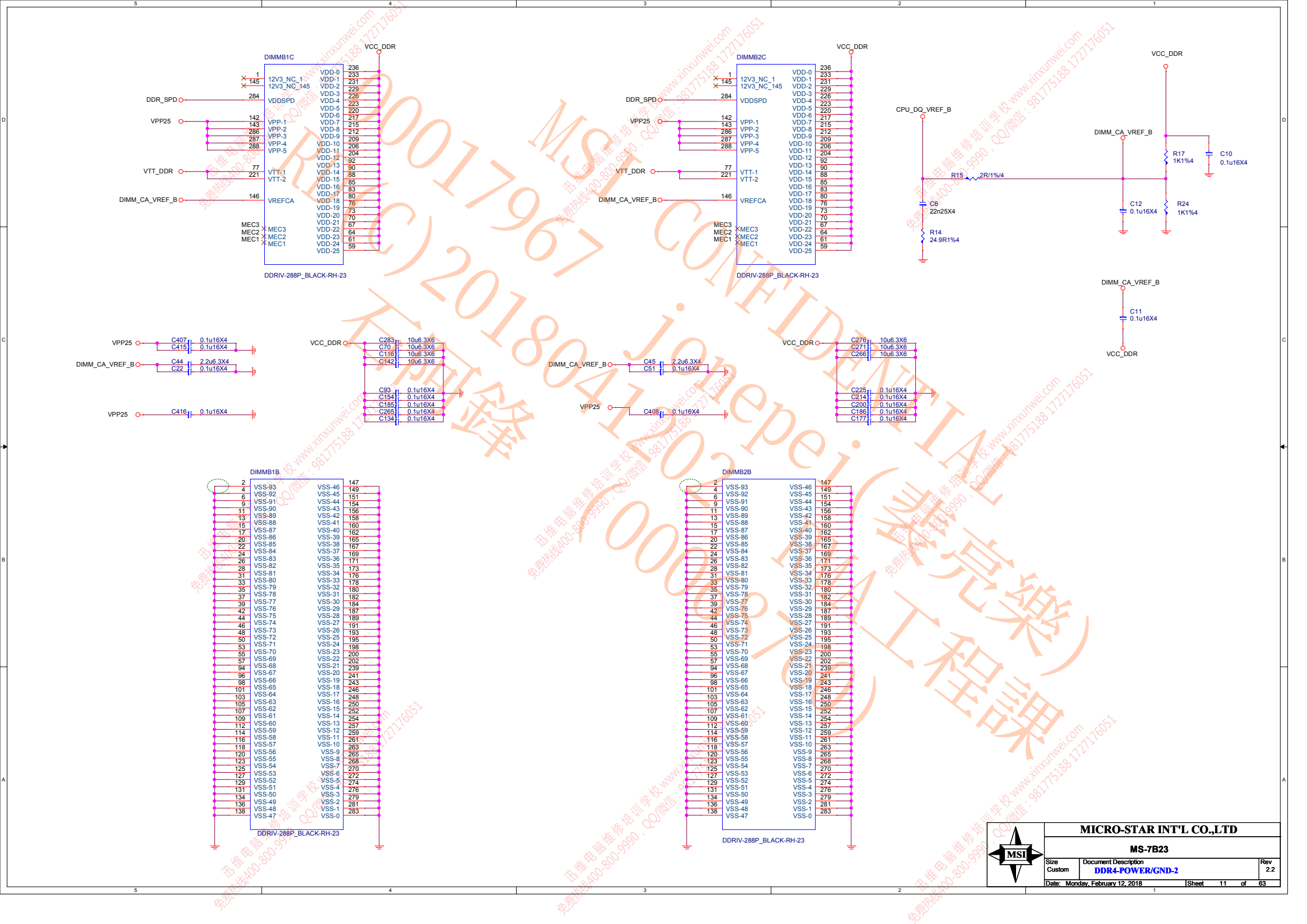
DIMMB1C
DDRIV-288P_BLACK-RH-23
VCC_DDR
DDR_SPD
VPP25
VTT_DDR
DIMM_CA_VREF_B
12V3_NC_1
12V3_NC_145
VDDSPD
VPP-1
VPP-2
VPP-3
VPP-4
VPP-5
VTT-1
VTT-2
VREFCA
MEC3
MEC2
MEC1
DIMMB2C
DDRIV-288P_BLACK-RH-23
CPU_DQ_VREF_B
R15 2R/1%/4
C6 22n25X4
R14 24.9R1%4
DIMM_CA_VREF_B
R17 1K1%4
C10 0.1u16X4
C12 0.1u16X4
R24 1K1%4
C11 0.1u16X4
C407 0.1u16X4
C415 0.1u16X4
C44 2.2u6.3X4
C22 0.1u16X4
C416 0.1u16X4
C283 10u6.3X6
C70 10u6.3X6
C116 10u6.3X6
C142 10u6.3X6
C93 0.1u16X4
C154 0.1u16X4
C185 0.1u16X4
C265 0.1u16X4
C134 0.1u16X4
C45 2.2u6.3X4
C51 0.1u16X4
C408 0.1u16X4
C276 10u6.3X6
C271 10u6.3X6
C266 10u6.3X6
C225 0.1u16X4
C214 0.1u16X4
C200 0.1u16X4
C186 0.1u16X4
C177 0.1u16X4
DIMMB1B
DDRIV-288P_BLACK-RH-23
DIMMB2B
DDRIV-288P_BLACK-RH-23
MICRO-STAR INT'L CO.,LTD
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Size
Custom
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DDR4-POWER/GND-2
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2017.12.07 Eric mail

VCC3 / 3VSB
R785 X 10K/4 LFRAME_CS0_N
R2113 X 10K/4
R965 X 10K/4 SERIRQ
R2112 10K/4
R774 X 10K/4 KBRST#_R
R2111 10K/4
R952 10K/4 PIRQA#
R2117 X 10K/4 LDRQ#_RST_N
R2118 X 10K/4

LPC_ESPI_IO0_R C1884 X 10p50N4
LPC_ESPI_IO1_R C1885 X 10p50N4
LPC_ESPI_IO2_R C1886 X 10p50N4
LPC_ESPI_IO3_R C1887 X 10p50N4
close to PCH in 500-1000mil

3VSB
R484 1K/4 SMBCLK_VSB_R
R485 1K/4 SMBDATA_VSB_R
R772 4.7K/4 SMBCLK_VSB
R771 4.7K/4 SMBDATA_VSB
LANPHY USE by SPEC
R730 499R1%4 SMLINK0_CLK
R731 499R1%4 SMLINK0_DATA
R783 1K/4 SMLINK1_CLK
R782 1K/4 SMLINK1_DATA

for loadline disable
3VSB R605 10K/4 GPP_H19

3VSB
R917 10K/4 GPP_H18
R606 10K/4 GPP_H17
R919 X 10K/4 GPP_H16
ID
R920 X 10K/4 GPP_H18
R604 X 10K/4 GPP_H17
R921 10K/4 GPP_H16

22,55 LPC_ESPI_IO0_R R950 0R/4 LPC_ESPI_IO0 BB39
22,55 LPC_ESPI_IO1_R R951 0R/4 LPC_ESPI_IO1 AW37
22,55 LPC_ESPI_IO2_R R953 0R/4 LPC_ESPI_IO2 AV37
22,55 LPC_ESPI_IO3_R R957 0R/4 LPC_ESPI_IO3 BA38
22,55 LFRAME_CS0_N LFRAME_CS0_N BE38
22,55 SERIRQ SERIRQ AW35
PIRQA# BA36
To SIO 22 KBRST# R786 0R/4 KBRST#_R BE39
22 LDRQ#_RST_N R738 X 0R/4 ESPI_RST# BF38
12,19,20,21 SMBCLK_VSB_R R781 X 0R/4 SMBCLK_VSB BE26
12,19,20,21 SMBDATA_VSB_R R770 X 0R/4 SMBDATA_VSB BF26
18 ME_TLS_ON ME_TLS_ON BE25
24 SMLINK0_CLK SMLINK0_CLK BF25
24 SMLINK0_DATA SMLINK0_DATA BE24
18 LPC_ESPI_SEL LPC_ESPI_SEL BF24
22 SMLINK1_CLK SMLINK1_CLK BF27
22 SMLINK1_DATA SMLINK1_DATA BE27
18 PCH_SML1ALERT# PCH_SML1ALERT# BD33
GPP_H12 AE48
AD47
AB47
18 GPP_H12 AF47
32 BIOS_SEL_PCIESATA1 AD48
32 BIOS_DIS_SW1 AC47
18 GPP_H15 GPP_H15 AE43
GPP_H16 AJ46
GPP_H17 AE44
GPP_H18

FAN MODE USE
25 CPUFAN1_MODE BF23
BC22
25 SYSFAN1_MODE BF21
26 SYSFAN2_MODE BE21
PWM LL disable 44 GPP_H19 GPP_H19 AH46
EZ LED 56 GPP_H20 GPP_H20 AG45
EZ LED 56 GPP_H21 GPP_H21 AH48
EZ LED 56 GPP_H22 GPP_H22 AH47
EZ LED 56 GPP_H23 GPP_H23 AJ47
AR2
AT5
AU4
41 PCH_CLK PCH_CLK AW47
41 PCH_MISO BA45
18,41 PCH_MOSI AU41
18,41 PCH_IO2 AY48
18,41 PCH_IO3 BA46
41 PCH_SPI_CS0# PCH_SPI_CS0# AY47
AW48
AT40
BF19
BE19
BE18
BF18
BD17
BC17
R2390 100K/4 PCH_CLK
2018.01.23 Robert mail

PCH1A
LPC eSPI
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#
SMB
GPP_H10/SML2CLK
GPP_H11/SML2DATA
GPP_H12/SML2ALERT#
GPP_H13/SML3CLK
GPP_H14/SML3DATA
GPP_H15/SML3ALERT#
GPP_H16/SML4CLK
GPP_H17/SML4DATA
GPP_H18/SML4ALERT#
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H20/ISH_I2C0_SCL
GPP_H21/ISH_I2C1_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H23/TIME_SYNC0
CL_CLK
CL_DATA
CL_RST#
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#
SPI JTAG
GPP_D0/SPI1_CS#/SBK0/BK0
GPP_D1/SPI1_CLK/SBK1/BK1
GPP_D2/SPI1_MISO/SBK2/BK2
GPP_D3/SPI1_MOSI/SBK3/BK3
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
PCH_H

Power Management
SLP_SUS# BD39 SLP_SUS# SLP_SUS# 22,23,54
SLP_A# BE40 SLP_A# TP16
SLP_S3# R787 0R/4 SLP_S3# BF42 SLP_S3# 15,22,38,42,50,51,54
SLP_S4# R761 0R/4 SLP_S4# BE42 SLP_S4# 15,22,38,42,49,50,51
SLP_S5# BC42 SLP_S5# SLP_S5# 15
SLP_S0# BC28 SLP_S0# TP52
SLP_LAN# BF40 SLP_LAN# SLP_LAN# 24
LAN_DISABLE# BF41 LAN_DISABLE# LAN_DISABLE# 24
GPD9/SLP_WLAN# BD42
GPP_A13/SUSWARN#/SUSPWRDNACK BC37 SUSWARN# R734 0R/4 CHIP_PWGD_SPI 41
GPP_A15/SUSACK# BE35 SUSACK#
GPD8/SUSCLK BE45 PCH_SUSCLK
R795 0R/4
DSW_PWROK AW41 PCH_DPWROK
PCH_PWROK AY42 PCH_PWROK_R R942 0R/4 PCH_DPWROK 22
SYS_PWROK AU3 CHIP_PWGD_PCH R796 0R/4 PCH_PWROK 54
CPUPWRGD AE3 CPU_PWRGD_R R633 0R/4 CPU_PWRGD 3 CHIP_PWGD 22
RTCRST# BE47 RTCRST# RTCRST# 40,42,54
SRTCRST# BD46 SRTCRST#
RSMRST# BA47 RSMRST#
DRAM_RESET# BB46 DRAM_RESET# DRAM_RESET# 8
SYS_RESET# AU2 FP_RST# FP_RST# 55
PLTRST_CPU# AG5 CPURST# CPURST# 3
GPP_B13/PLTRST# AV29 PLTRST#_R R946 30R1%4 PLTRST# 22
GPD3/PWRBTN# BE46 PWRBTN# PWRBTN# 22
WAKE# BB47 SB_WAKE# SB_WAKE# 19,20,21,32,33
GPD2/LAN_WAKE# BG44 LANPHY_WAKE# LANPHY_WAKE# 24
GPP_A11/PME#/SD_VDD2_PWR_EN# BE36 IO_PME_N IO_PME_N 22
GPD1/ACPRESENT BG42 ACPRESENT
GPD0/BATLOW# BF44 BATLOW#
GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF# BF36 GPP_A12
GPP_A8/CLKRUN# AV32 PCH_CLKRUN#
PECI AF2 PCH_PECI R648 X 0R/4 CPU_PECI 3,22
THRMTRIP# AD3 PCH_THERMTRIP_R R626 619R/1%4 PCH_THERMTRIP# 3
PM_DOWN AE2 CPU_PM_DOWN 3
PM_SYNC AF3 SYNC_R R634 30R1%4 CPU_PM_SYNC 3
INTRUDER# BB44 INTRUDER#
Place R390 within 200mil of PCH.

STRAP
GPP_B14/SPKR AW29 SPKR SPKR 18,55
GPP_B18/GSPI0_MOSI BE30 NO_REBOOT NO_REBOOT 18
GPP_B22/GSPI1_MOSI BA26 BOOT_BIOS_SEL BOOT_BIOS_SEL 18
GPD7 BE41 GPD7 18

PCH_JTAG_TCK AJ3
PCH_JTAG_TMS AJ4 XDP_TMS 3
PCH_JTAG_TDI AH2 XDP_TDI 3
PCH_JTAG_TDO AH3 XDP_TDO 3
PCH_JTAGX AH4 XDP_TCK0 3
ITP_PMODE AL3 ITP_PMODE TP13
TRIGGER_IN AK2
TRIGGER_OUT AK3 PCH_TRIGOUT R652 30R/4 CPU_OUTPUT_TRIGGER 3
PREQ# AL2 CPU_INPUT_TRIGGER 3
PRDY# AM5 CPU_PREQ 3
CPU_TRST# AM4 CPU_PRDY 3
XDP_TRST 3

PCH LANPHY PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
LAN_DISABLE# R759 X 10K/4
SB_WAKE# R762 1K/4 3VDSW
LANPHY_WAKE# R788 4.7K/4
PWRBTN# R956 3K1%4
BATLOW# R737 10K/4
ACPRESENT R760 X 10K/4
SLP_S3# R2392 X 10K/4
SLP_S4# R2393 X 10K/4
2018.01.23 Robert mail
SLP_S3# R2389 100K/4
SLP_S4# R2388 100K/4
SLP_LAN# R2391 100K/4
PCH_SUSCLK R941 X 1.5K/4

PCH_CLKRUN# R945 X 10K/4 3VSB
2017.12.07 Eric mail
CRB RSVD pull up to +V3P3_DUAL.

IO_PME_N R756 10K/4 3VSB
SUSACK# R755 X 10K/4 3VSB
GPP_A12 R735 X 10K/4 3VSB
PCH_PECI R650 X 1K/4
CPU_PM_DOWN R632 X 51R/4
FP_RST# R719 1K/4 VCC3

Defensive Termination. CRB unstuff.
Place within 1.1" of PCH Pin.
VCCSTPLL
XDP_TCK0 R649 X 1K/4
XDP_TMS R653 51R/4
XDP_TDO R635 100R1%4
XDP_TDI R651 51R/4
Place within 1.5" of PCH Pin.

PCH_JTAG_TCK R636 X 51R/4
Defensive Termination. CRB unstuff.
Place within 1.1" of PCH Pin.

RSMRST# USE solution

2017.08.14 Eric mail add
2017.11.30 Robert mail remove

RSMRST#
3VSB R800 4.7K/4
RSMRST# R789 X 0R/4 SIO_RSMRST# 22,41
R997 0R/4 RSMRST#_SLG 54
R801 100K/4

擺在一起(注意到所有的SMBUS的分支)

SMBCLK_VCC R798 4.7K/4
SMBDATA_VCC R779 4.7K/4 VCC3
3VSB R753 10K/4
+12V R750 10K/4
CFL CRB
PCH_PWROK R749 0R/4 PCH_PWROK_SMBUS
R748 100K/4
Q88 NN-2N7002D
59G
SMBCLK_VSB
Q93 2N7002 R797 X_0R/4
SMBCLK_VSB SMBCLK_VSB 35,36,37,49
SMBCLK_VCC SMBCLK_VCC 8
SMBDATA_VSB
Q92 2N7002 R780 X_0R/4
SMBDATA_VSB SMBDATA_VSB 35,36,37,49
SMBDATA_VCC SMBDATA_VCC 8

SMBUS ESD

D18 X_ESD-AOZ8231 SMBCLK_VSB_R 12,19,20,21
D17 X_ESD-AOZ8231 SMBDATA_VSB_R 12,19,20,21
close to PCH

RTC

VBAT_PCH
2014.12.29
CRB R763 20K1%4
SRTCRST#
C623 1u16X6
2017.12.20 remove RTC

Chassis Intrusion

VBAT_PCH
R738 1M/4
JCI1 H1X2M_BLACK-RH
INTRUDER#
D19 X_ESD-AOZ8231

MICRO-STAR INT'L CO.,LTD
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RTC Block

Close to PCH

C596 12p50N6 RTCX2
Y2
R703 10M/6 <1 inch
RTCX1
C595 12p50N6
32.768KHZ12.5p_D-RH-10

XTAL_24M_PCH_OUT
R615 200K1%4 XTAL_24M_PCH_IN
PDG
R613 0R/4
24M_OUT R612 0R/4 24M_R
R614 0R/4
Y1 24MHZ20p
24M_IN
C539 18p50N4
C551 18p50N4
for 0A sa fail

C740 X_10p50N4
22 CLK_SIO_PCI R943 22R/4 CLK_PCH_LPC0 BB36
55 CLK_24M_TPM R954 15R1%4 CLK_PCH_24M BB34
C1888 X_10p50N4
2017.12.07 Eric mail
RTCX1 BA49
RTCX2 BA48
XCLK_BIASREF < 1000 mil
XTAL_24M_PCH_IN U10
XTAL_24M_PCH_OUT U9
R603 60.4R1%4 XCLK_BIASREF T3
R916 10K/4 R6
2017.08.23 Robert mail
TP18 SLOT1_CLKREQ#0 BF31
TP17 SLOT2_CLKREQ#1 BE31
TP49 SLOT3_CLKREQ#2 AR32
BB30
33 CLKREQ#4 CLKREQ#4 BA30
AN29
AE47
AC48
24 LAN_CLKREQ#9 AE41
AF48
AC41
AC39
AE39
AB48
AC44
32 CLKREQ#15 CLKREQ#15 AC43

PCH1E
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
LPC
RTCX1
RTCX2
RTC
XTAL_IN
XTAL_OUT
XCLK_BIASREF
24MHZ
CLKIN_XTAL
GPP_B5/SRCCLKREQ0#
GPP_B6/SRCCLKREQ1#
GPP_B7/SRCCLKREQ2#
GPP_B8/SRCCLKREQ3#
GPP_B9/SRCCLKREQ4#
GPP_B10/SRCCLKREQ5#
CLK_REQ
GPP_H0/SRCCLKREQ6#
GPP_H1/SRCCLKREQ7#
GPP_H2/SRCCLKREQ8#
GPP_H3/SRCCLKREQ9#
GPP_H4/SRCCLKREQ10#
GPP_H5/SRCCLKREQ11#
GPP_H6/SRCCLKREQ12#
GPP_H7/SRCCLKREQ13#
GPP_H8/SRCCLKREQ14#
GPP_H9/SRCCLKREQ15#
PCH_H

CLKOUT_CPUBCLK_P B8 PCH_CPU_BCLK_DP → PCH_CPU_BCLK_DP 3
CLKOUT_CPUBCLK_N C8 PCH_CPU_BCLK_DN → PCH_CPU_BCLK_DN 3 100M
CLKOUT_CPUNSSC_P D7 PCH_CPU_NSSC_CLK_DP → PCH_CPU_NSSC_CLK_DP 3
CLKOUT_CPUNSSC_N C6 PCH_CPU_NSSC_CLK_DN → PCH_CPU_NSSC_CLK_DN 3 24M
CLKOUT_CPUPCIBCLK_P A6 PCH_CPU_PCIE_DP → PCH_CPU_PCIE_DP 3
CLKOUT_CPUPCIBCLK_N B6 PCH_CPU_PCIE_DN → PCH_CPU_PCIE_DN 3 100M
CLKOUT_ITPXDP_P Y4
CLKOUT_ITPXDP_N Y3

CLKOUT_PCIE_P0 AJ7 CK_SLOT1_DP → CK_SLOT1_DP 19
CLKOUT_PCIE_N0 AJ6 CK_SLOT1_DN → CK_SLOT1_DN 19
CLKOUT_PCIE_P1 AH10 CK_SLOT2_DP → CK_SLOT2_DP 20
CLKOUT_PCIE_N1 AH9 CK_SLOT2_DN → CK_SLOT2_DN 20
CLKOUT_PCIE_P2 AE15 CK_SLOT3_DP → CK_SLOT3_DP 20
CLKOUT_PCIE_N2 AE14 CK_SLOT3_DN → CK_SLOT3_DN 20
CLKOUT_PCIE_P3 AE7 CK_SLOT4_DP → CK_SLOT4_DP 21
CLKOUT_PCIE_N3 AE6 CK_SLOT4_DN → CK_SLOT4_DN 21
CLKOUT_PCIE_P4 AC3 CLK_M2_2_DP → CLK_M2_2_DP 33
CLKOUT_PCIE_N4 AC2 CLK_M2_2_DN → CLK_M2_2_DN 33
CLKOUT_PCIE_P5 AB3
CLKOUT_PCIE_N5 AB2
CLKOUT_PCIE_P6 W3
CLKOUT_PCIE_N6 W4
CLKOUT_PCIE_P7 W6
CLKOUT_PCIE_N7 W7
CLKOUT_PCIE_P8 AC15
CLKOUT_PCIE_N8 AC14
CLKOUT_PCIE_P9 U3 CLK_LAN_DP → CLK_LAN_DP 24
CLKOUT_PCIE_N9 U2 CLK_LAN_DN → CLK_LAN_DN 24
CLKOUT_PCIE_P10 AC11
CLKOUT_PCIE_N10 AC9
CLKOUT_PCIE_P11 AE11
CLKOUT_PCIE_N11 AE9
CLKOUT_PCIE_P12 AC6
CLKOUT_PCIE_N12 AC7
CLKOUT_PCIE_P13 Y2
CLKOUT_PCIE_N13 AA1
CLKOUT_PCIE_P14 T1
CLKOUT_PCIE_N14 T2
CLKOUT_PCIE_P15 V3 CLK_M2_1_DP → CLK_M2_1_DP 32
CLKOUT_PCIE_N15 V2 CLK_M2_1_DN → CLK_M2_1_DN 32

3VSB
R598 10K/4 LAN_CLKREQ#9
R918 10K/4 CLKREQ#15
VCC3
R947 10K/4 CLKREQ#4
2017.11.07 Robert mail
Optance pu to VCC3

EMI
AZ_BITCLK
C602 X_10p50N4

27 AZ_SDIN0 AZ_SDIN0 BE11
BF10
18 AZ_SDOUT_R AZ_SDOUT_R
27 AZ_SDOUT AZ_SDOUT R724 33R/4 AZ_SDOUT_R BF12
27 AZ_BITCLK AZ_BITCLK R723 33R/4 AZ_BITCLK_LR BD11
27 AZ_RST# AZ_RST# R722 33R/4 AZ_RST#_R BE10
27 AZ_SYNC AZ_SYNC R725 33R/4 AZ_SYNC_R BG13

PCH1D
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_SDO/I2S0_TXD
HDA_BCLK/I2S0_SCLK
HDA_RST#/I2S1_SCLK
HDA_SYNC/I2S0_SFRM
AUDIO
HDACPU_SDO
HDACPU_SDI
HDACPU_SCLK
I2S1_TXD/SNDW2_DATA
I2S1_SFRM/SNDW2_CLK
GPP_D5/I2S2_SFRM/CNV_RF_RESET#
GPP_D6/I2S2_TXD/MODEM_CLKREQ
GPP_D7/I2S2_RXD
GPP_D8/I2S2_SCLK
GPP_D17/DMIC_CLK1/SNDW3_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D20/DMIC_DATA0/SNDW4_DATA
PCH_H

3 PCH_CPU_AUD_SDO R677 30R/4 PCH_CPU_AUD_SDO_R AM2
3 PCH_CPU_AUD_SDI PCH_CPU_AUD_SDI_R AN3
3 PCH_CPU_AUD_SCLK R675 30R/4 PCH_CPU_AUD_SCLK_R AM3

Default Native F3/CNV_RF_R_ESET#.
TP57 BE12
TP53 BD12
Default Native F3/MODEM_CLKREQ.
BE16
BA17
AW18
AV18
AW15
AV16
BD16
BF15

PORT B
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I0/DDPB_HPD0/DISP_MISC0
PORT C
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I1/DDPC_HPD1/DISP_MISC1
PORT D
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_I2/DPPD_HPD2/DISP_MISC2
PORT F
GPP_F22/DDPF_CTRLCLK
GPP_F23/DDPF_CTRLDATA
eDP
GPP_F19/EDP_VDDEN
GPP_F20/EDP_BKLTEN
GPP_F21/EDP_BKLTCTL
GPP_I4/EDP_HPD/DISP_MISC4
GPP_I3/DPPE_HPD3/DISP_MISC3

AL13 HDMI_DDPB_CTRLCLK → HDMI_DDPB_CTRLCLK 30
AR8 HDMI_DDPB_CTRLDATA → HDMI_DDPB_CTRLDATA 30
AT6 HDMI_DDPB_HPD SMI Pin → HDMI_DDPB_HPD 30
AN13 DVI_DDPC_CTRLCLK → DVI_DDPC_CTRLCLK 29
AL10 DVI_DDPC_CTRLDATA → DVI_DDPC_CTRLDATA 29
AN10 DVI_DDPC_HPD SMI Pin → DVI_DDPC_HPD 29
AL9 DSP_DDPD_CTRLCLK → DSP_DDPD_CTRLCLK 31
AR3 DSP_DDPD_CTRLDATA → DSP_DDPD_CTRLDATA 31
AP9 DSP_DDPD_HPD SMI Pin → DSP_DDPD_HPD 31
AT49 GPP_F22 → TP14
AN40 GPP_F23 → TP43
AV44
AV46
AU48
AN6 EDP_HPD R679 100K/4
AL15 DDPE_HPD3 R924 10K/4 SMI Pin

VCC3
HDMI_DDPB_CTRLCLK R700 2.2K/4
HDMI_DDPB_CTRLDATA R717 2.2K/4
DVI_DDPC_CTRLCLK R671 2.2K/4
DVI_DDPC_CTRLDATA R673 2.2K/4
DSP_DDPD_CTRLCLK R674 2.2K/4
DSP_DDPD_CTRLDATA R672 2.2K/4
DSP_DDPD_HPD R697 X_100K/4
改版視情況拿掉

DDI interfaace Disable
no connect

Port B HDMI

Port C DVI,HDMI2.0 OR Others

Port D DisplayPort to VGA

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MS-7B23
Size Custom
Document Description PCH-Audio/Display/Clock
Rev 2.2
Date: Monday, February 12, 2018 Sheet 13 of 63

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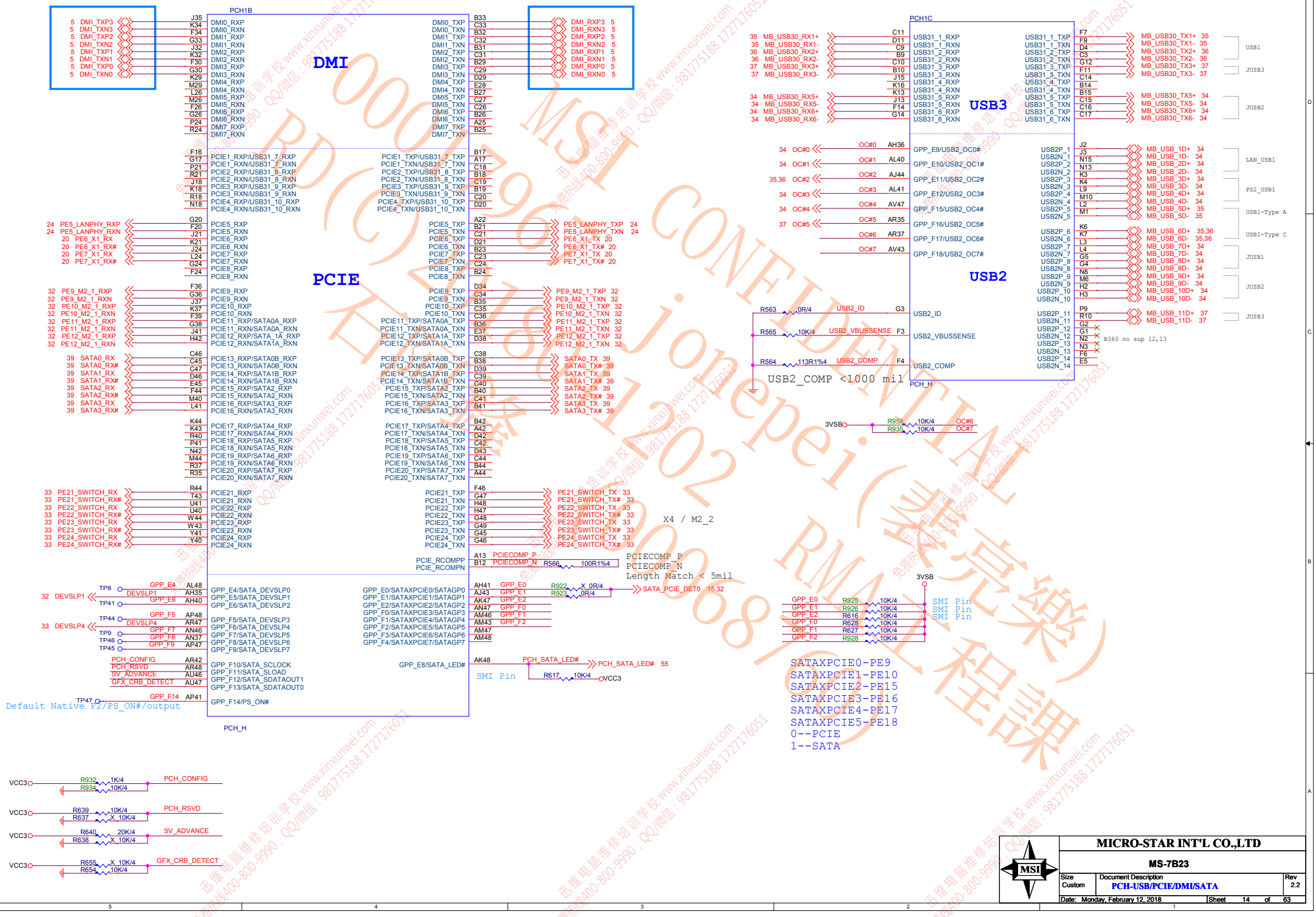
MSI CONFIDENTIAL RD(C)2018041202 Rui Wei(瑞威) 内部资料 00017967 (00066066)



MICRO-STAR INT'L CO.,LTD

MS-7B23

Size	Document Description	Rev
Custom	PCH-USB/PCIE/DMI/SATA	2.2

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MSI CONFIDENTIAL
RD(C)_Jonepei(樊完缴)_1802_00968(C)_RMA_程課
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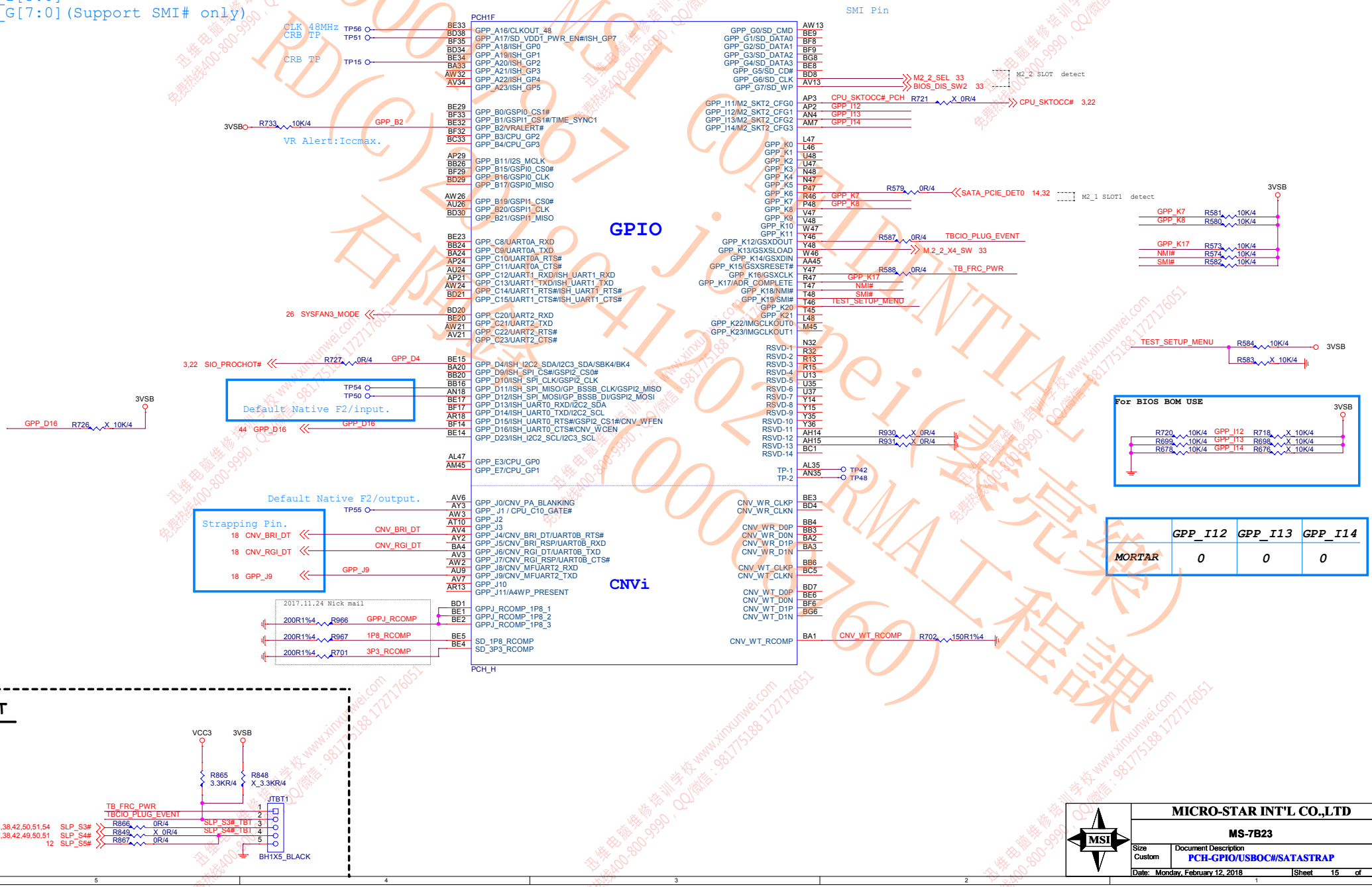
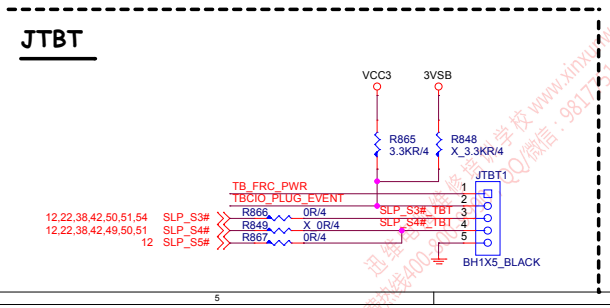
GPIO(SMI/NMI):
GPP_B14,GPP_B20,GPP_B23
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]
GPP_I[3:0]
GPP_G[7:0](Support SMI# only)



	GPP_I12	GPP_I13	GPP_I14
MORTAR	0	0	0



MICRO-STAR INT'L CO.,LTD	
MS-7B23	
Size: Custom	Document Description: PCH-GPIO/USBOC#/SATASTRAP
Rev: 2.2	
Date: Monday, February 12, 2018	Sheet 15 of 63

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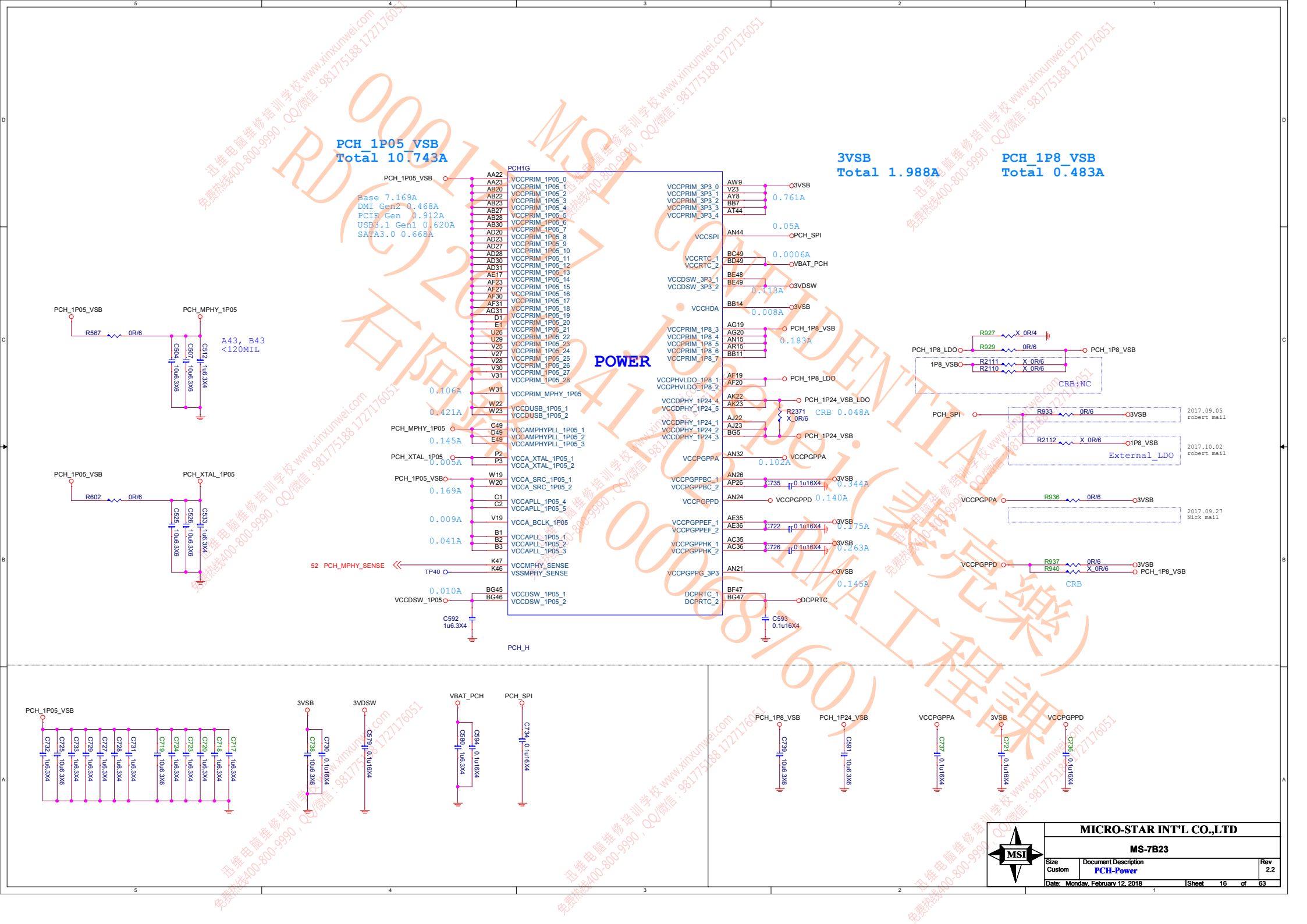
MSI CONFIDENTIAL 000196741 Jinpei(锦沛) 0000(760) RMA工程课 RD(完整版)



0091 MSI COMPUTER CORP. MS-7B23 1.0 B3D41 (2018/02/12 10:06:08)
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MICRO-STAR INT'L CO.,LTD	
MS-7B23	
Size: Custom	Document Description: PCH-Power
Rev: 2.2	
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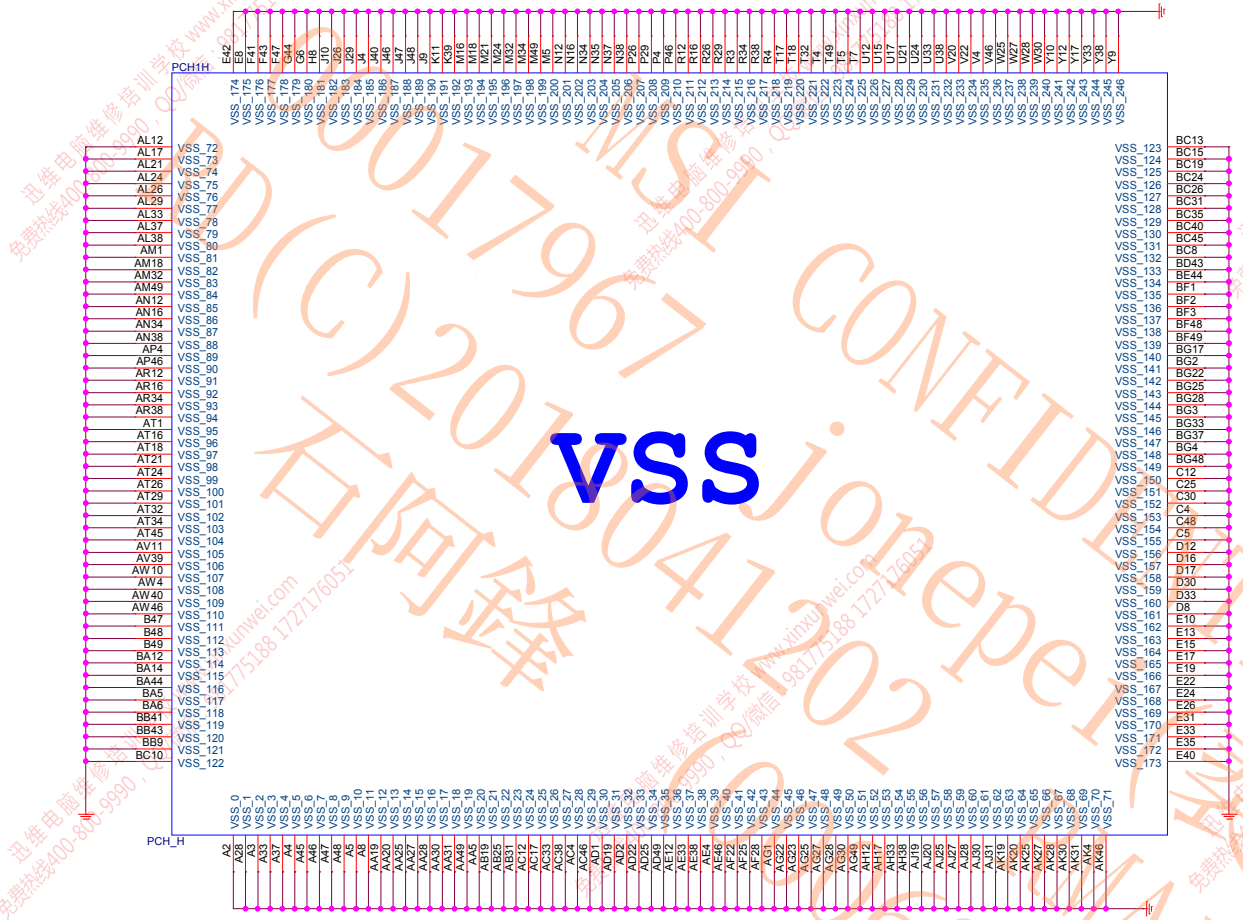

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Jonepe(完樂)
石阿鋒 EIA工程課

MICRO-STAR INT'L CO.,LTD	
MS-7B23	
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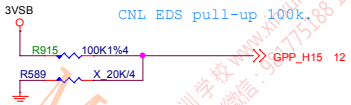
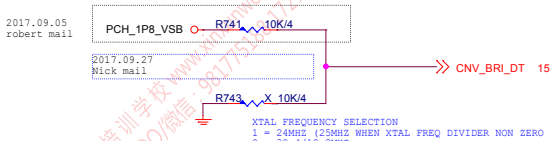
TOP Swap

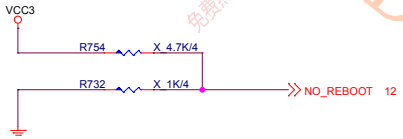
Internal pull-down 20K is disabled after PLTRST#

Reserved





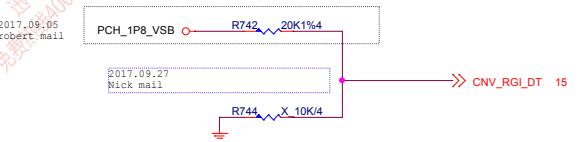
No Reboot



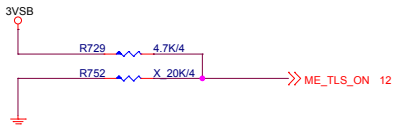
0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

Reserved



AMT and SBA with confidentiality

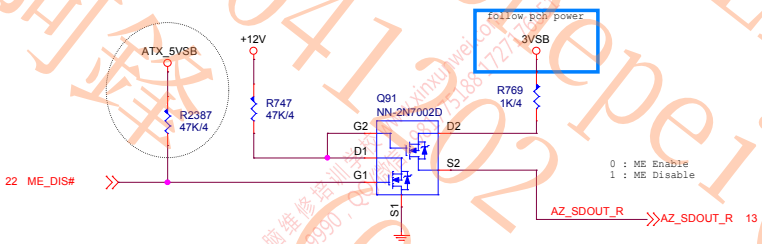


0 : DISABLE
1 : ENABLE (Default)

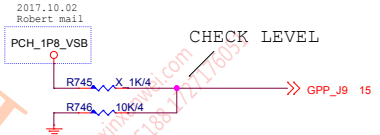
Internal pull-down 20K is disabled after RSMRST

HDA_SDO

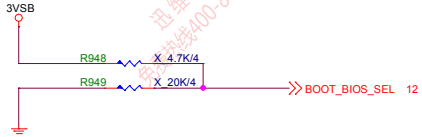
ME flash by GPIO



1.8V VCCSPI



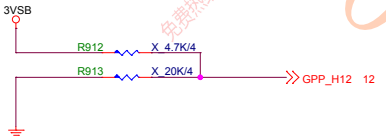
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

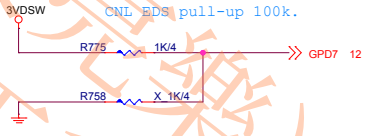
ESPI FLASH SHARING MODE



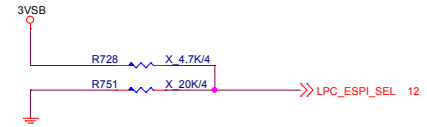
0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

Reserved



LPC eSPI Mode

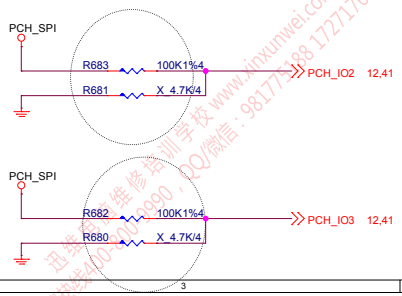


0 : LPC
1 : eSPI

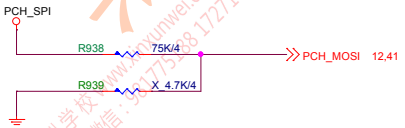
Internal pull-down 20K is disabled after RSMRST

Reserved

CRB 571506 Page.99

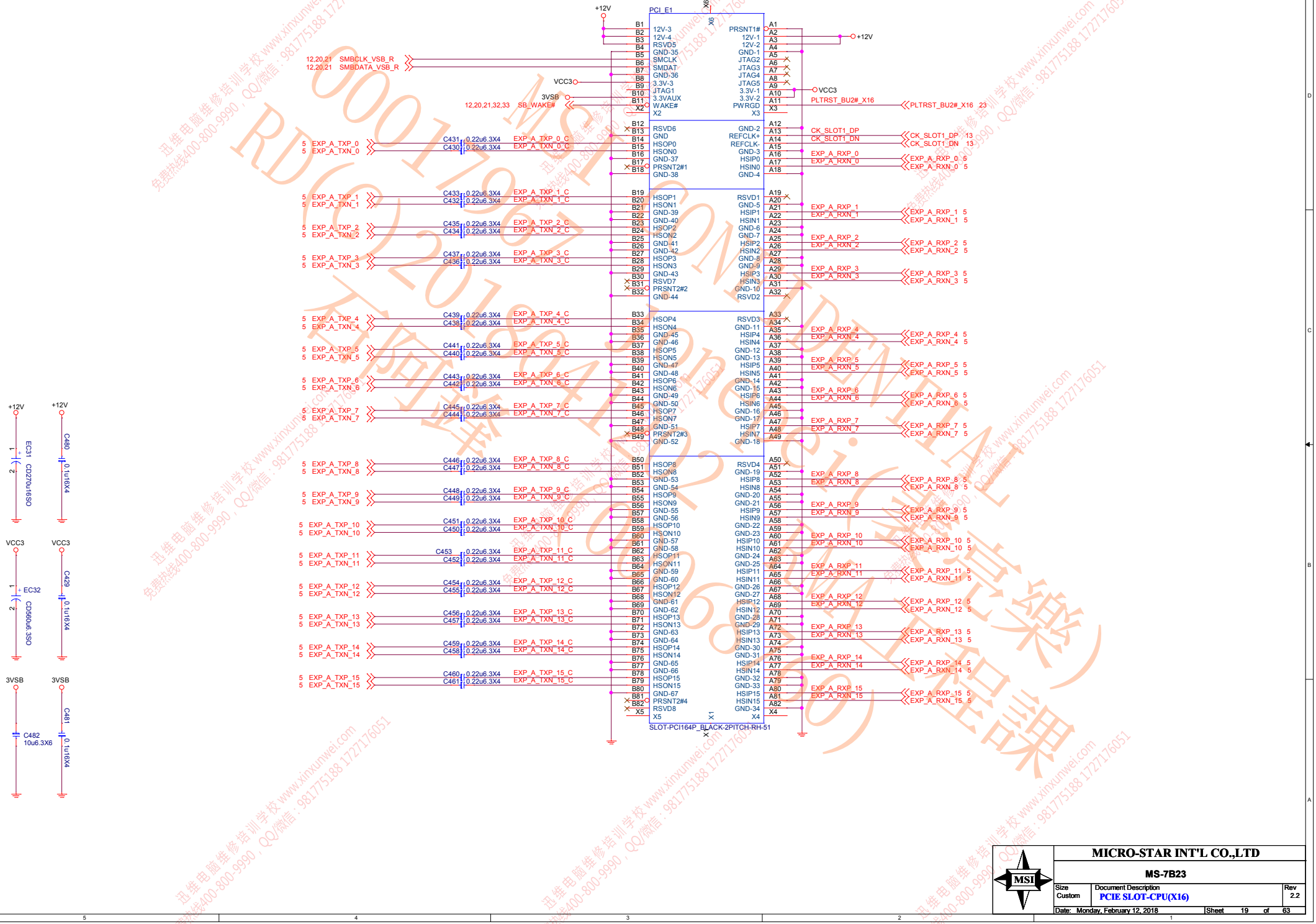


Reserved



MICRO-STAR INT'L CO.,LTD		
MS-7B23		
Size: Custom	Document Description: PCH-Strap	Rev: 2.2
Date: Monday, February 12, 2018	Sheet 18 of 63	

MSI CONFIDENTIAL jonepei(维修完成) RD(C)20180412 RMA(C)00068760 00017967 打印保存



MICRO-STAR INT'L CO.,LTD	
MS-7B23	
Size: Custom	Document Description: PCIE SLOT-CPU(X16)
Rev: 2.2	
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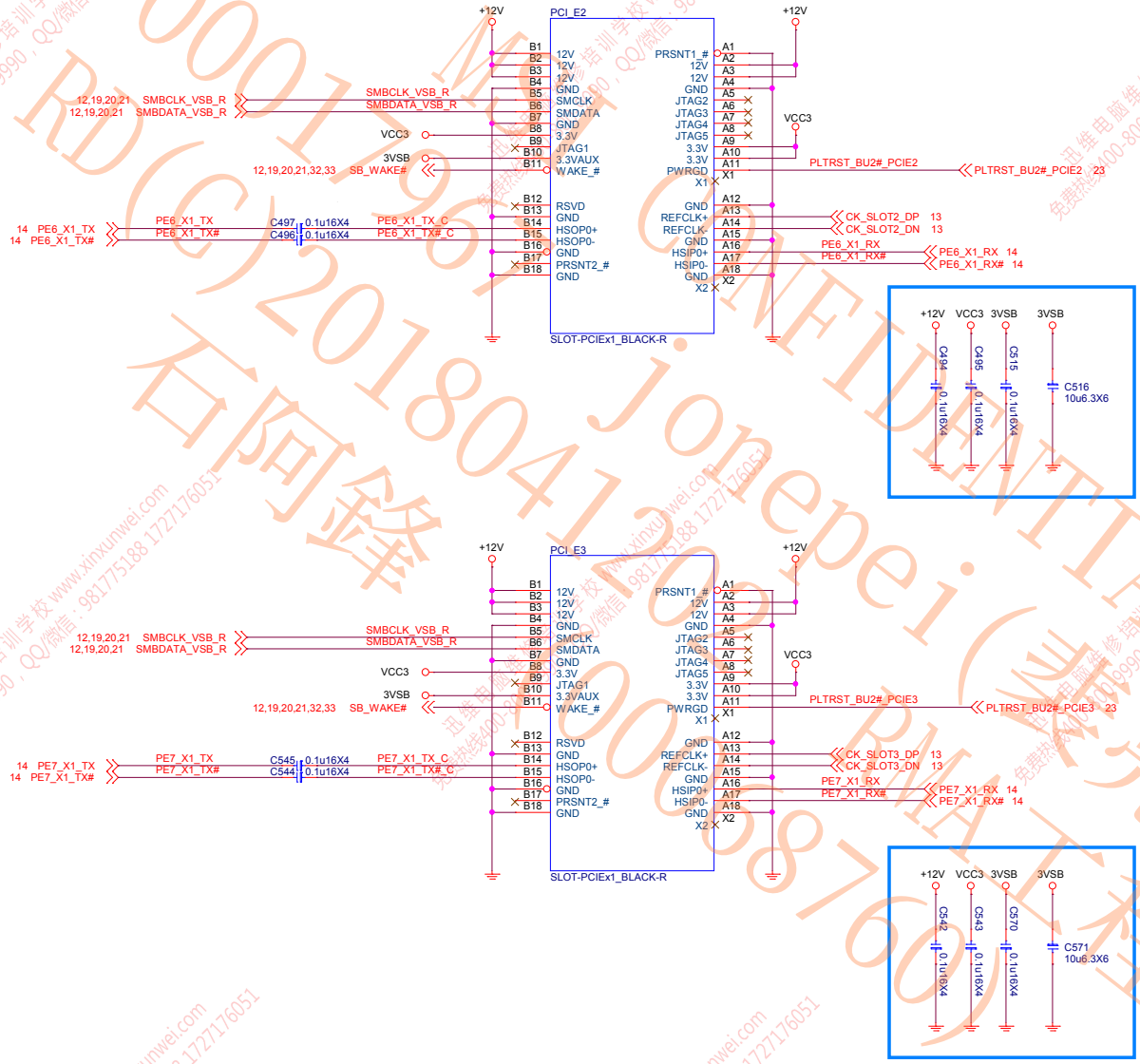

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Size: Custom | Document Description: PCIE SLOT-PCH(X1) | Rev: 2.2

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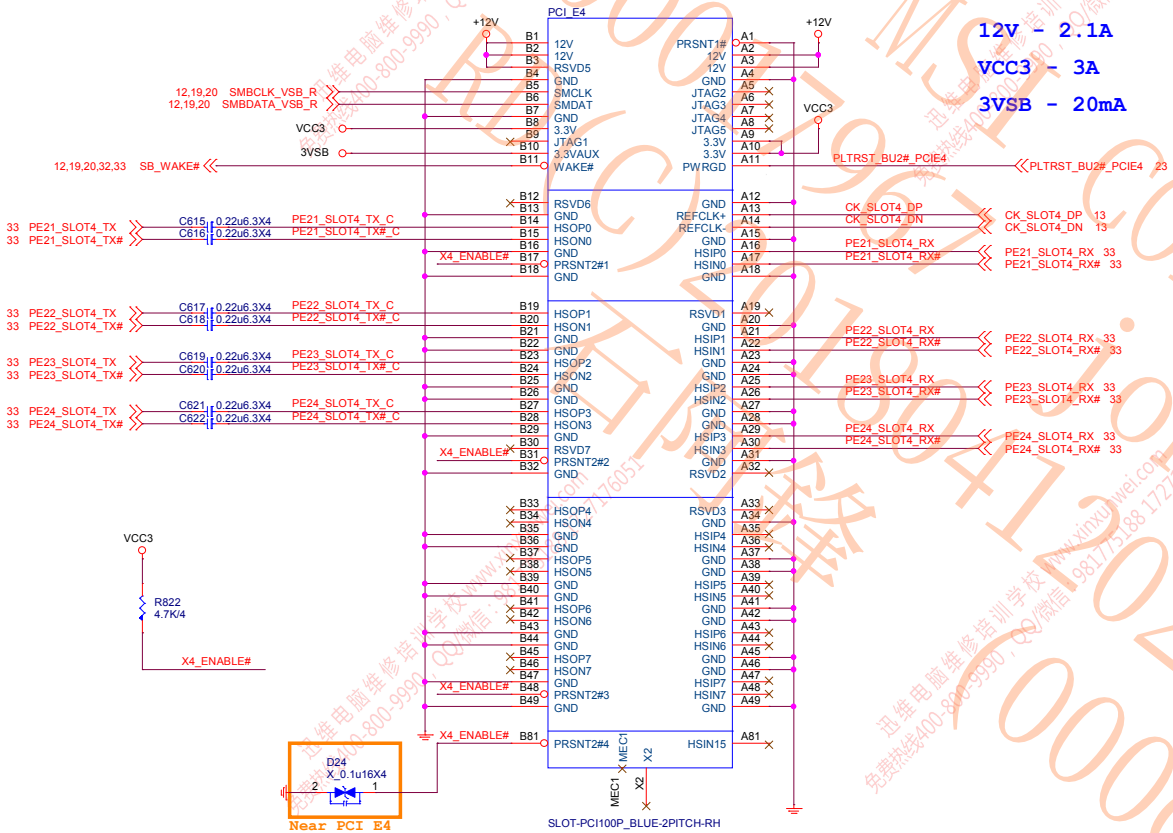
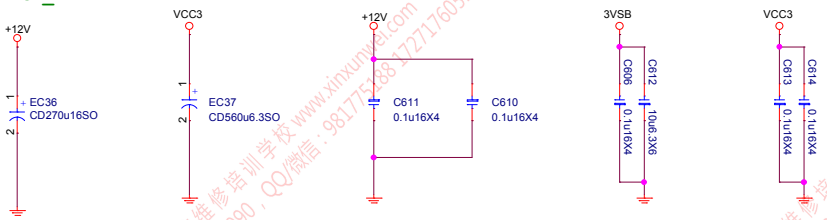
0001966 Jonepei(裁完缴) RD(C)20180412002 RMA工程课 00068760 石阿锋

PCI Express X4 Slot



Near PCI_E4



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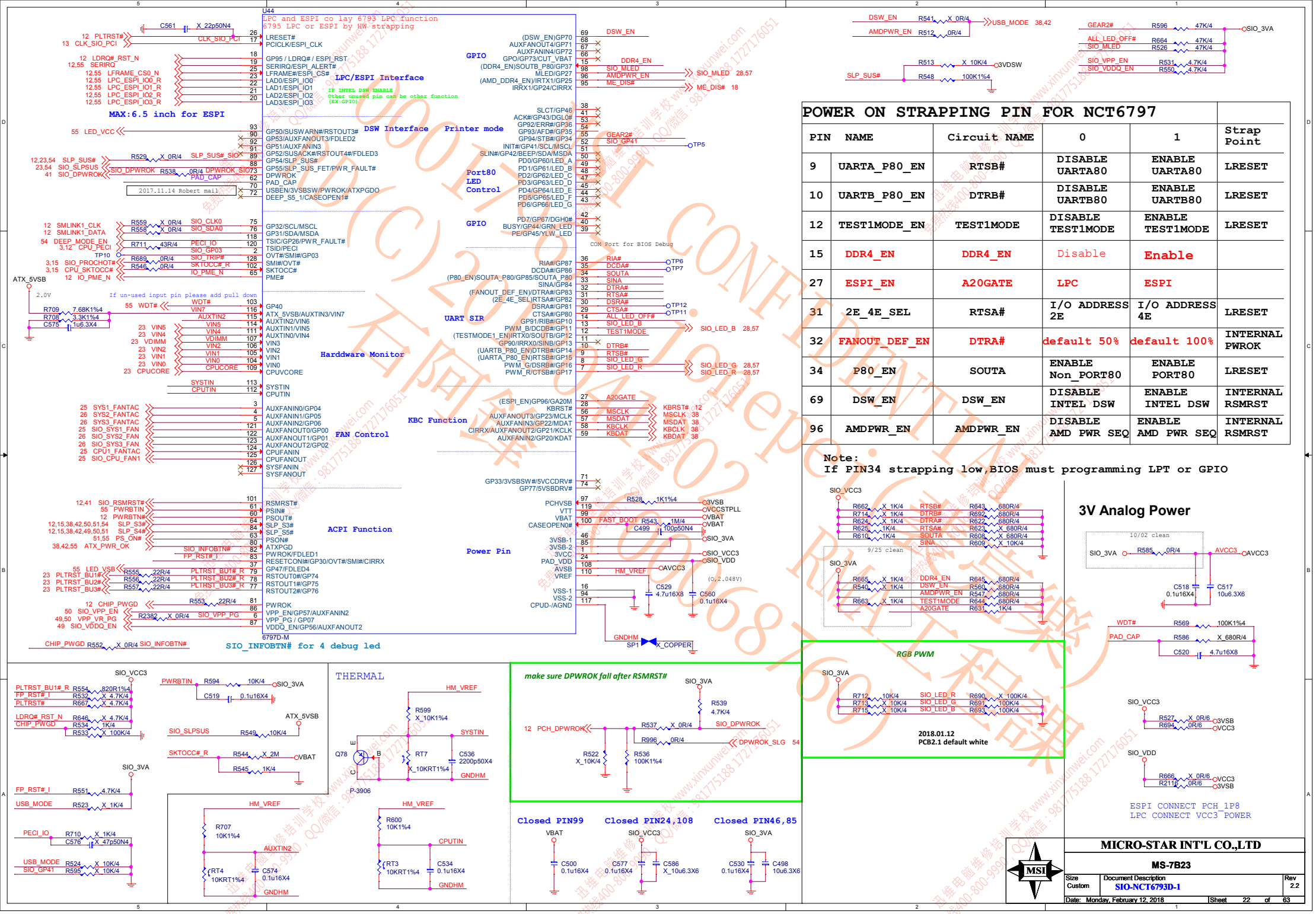
MS-7B23		
Size: Custom	Document Description: PCIE SLOT-PCH(X4)	Rev: 2.2
Date: Monday, February 12, 2018	Sheet 21 of 63	

MSI CONFIDENTIAL 000196741 202 RMA工程課 (000068760) 廣(C)01886 (樣完樂)



POWER ON STRAPPING PIN FOR NCT6797

PIN	NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	A20GATE	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

2018.01.12
PCB2.1 default white

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Size: Custom	Document Description: SIO-NCT6793D-1		Rev: 2.2
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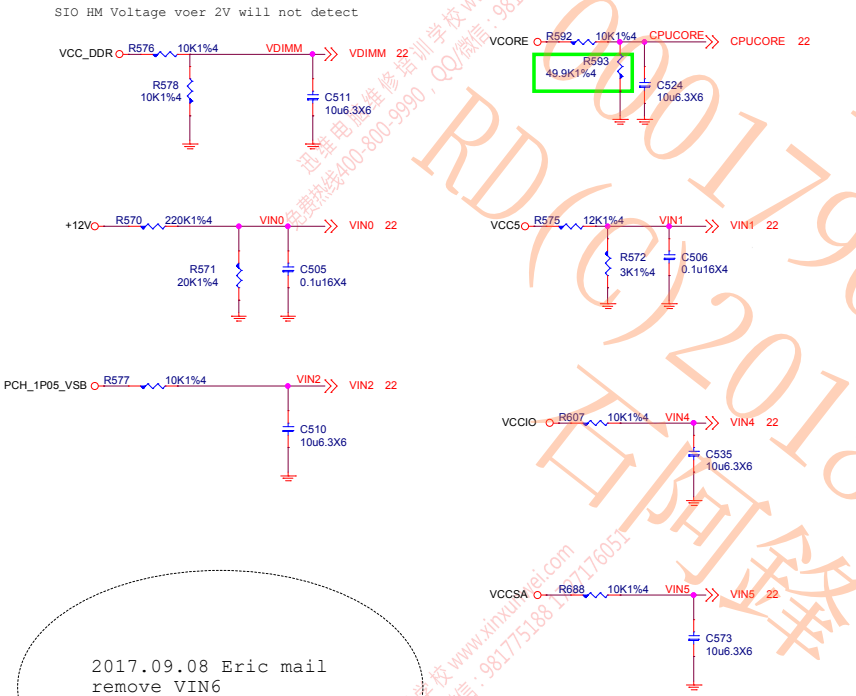
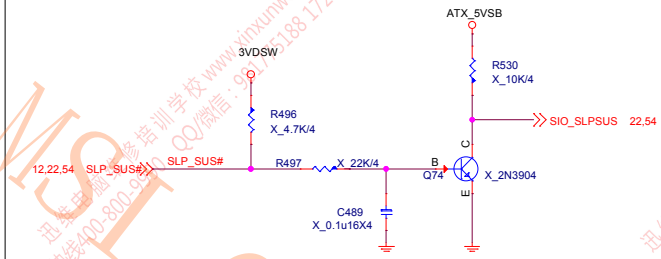
HW Monitor - Voltage



2017.09.08 Eric mail
remove VIN6
change to AUXTIN2

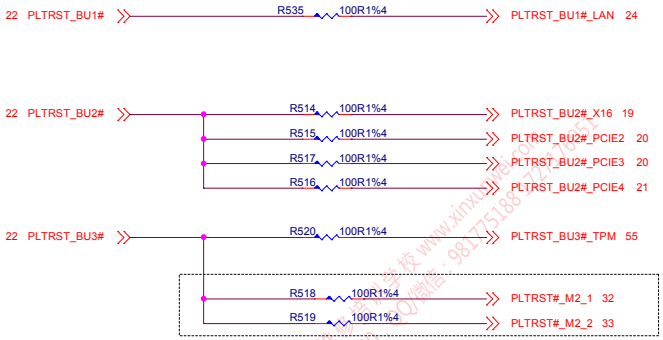
SLP_SUS Co-lay circuit



2017.09.25
remove for space

PLTRST#

oper drain for onboard chip



push pull for slots

SERIAL PORT 1

2017.09.25
remove JCOM1

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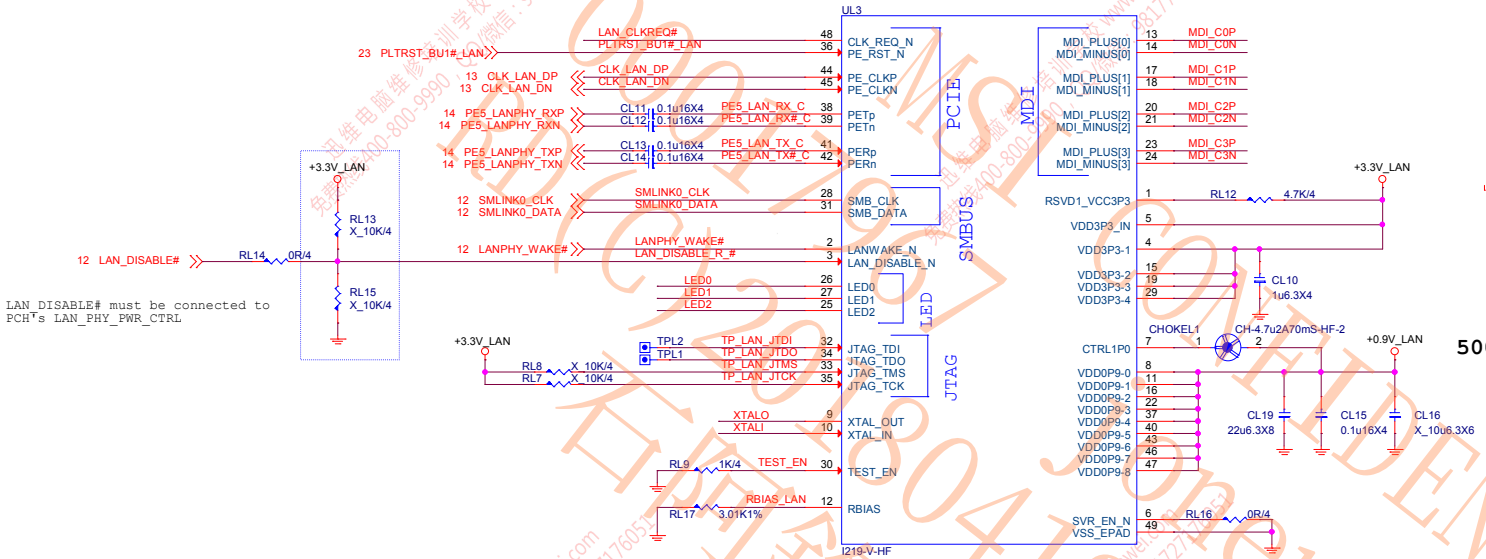
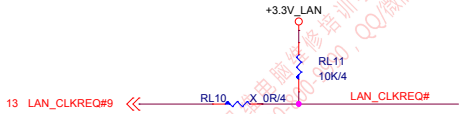
Intel Lan- i219

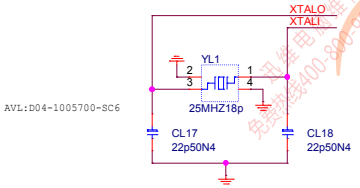
8111H:B06-08111CC-R09
8111G:B06-081116C-R09



LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL

PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN

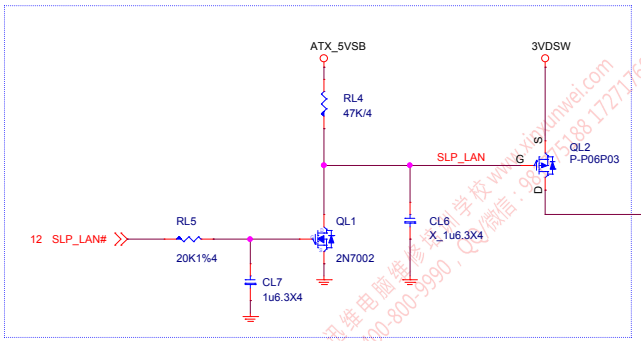


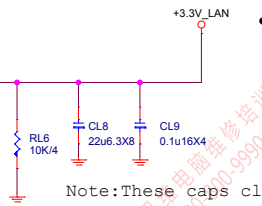


AVL:D04-1005700-SC6

The 10Kohm pull-up resistor (RL18) of CLK_REQ_N
is connected to 3.3V Suspend/Core/etc.
power well, depending on the power well
of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



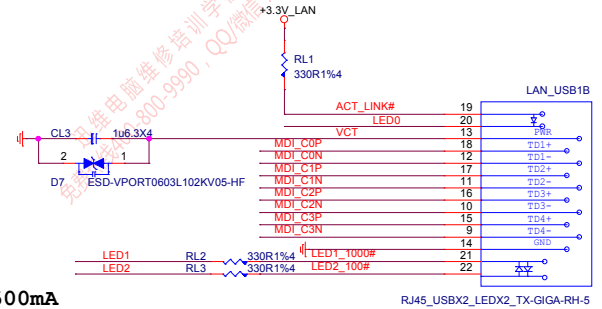


Note:These caps closed to PHY

+3.3V_LAN

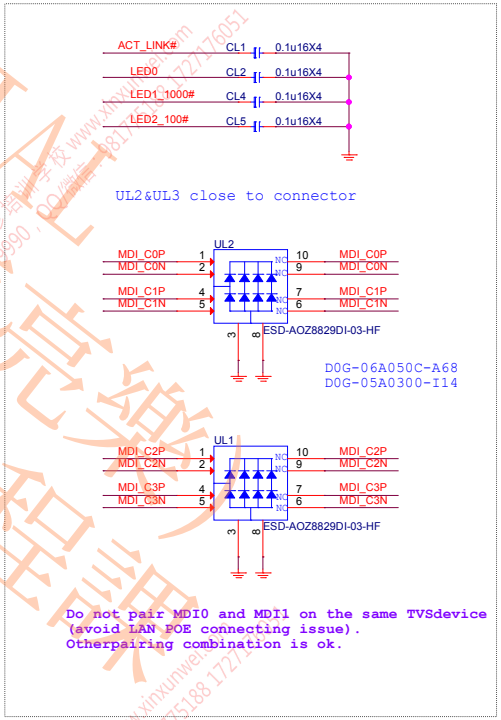
I218:132mA
I219:542mW

LAN Connector



500mA

For EMI



Do not pair MDI0 and MDI1 on the same TVSdevice (avoid LAN POE connecting issue).
Otherpairing combination is ok.

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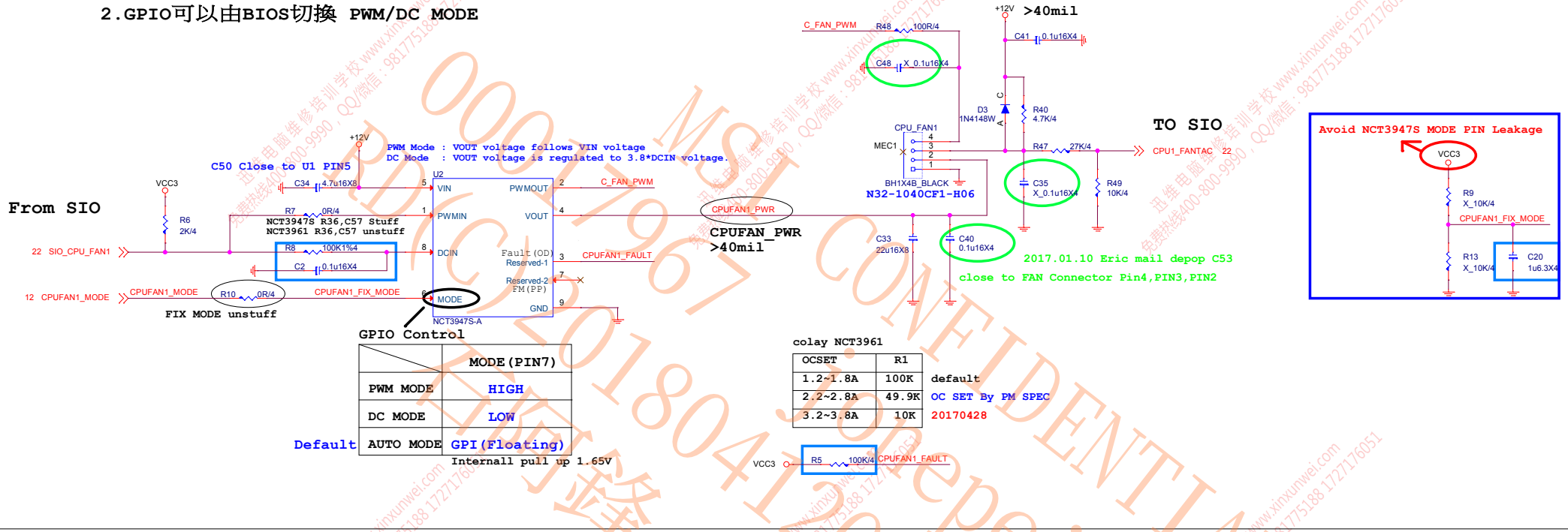
CONFIDENTIAL 仁寶(昆山)
RMA工程樣

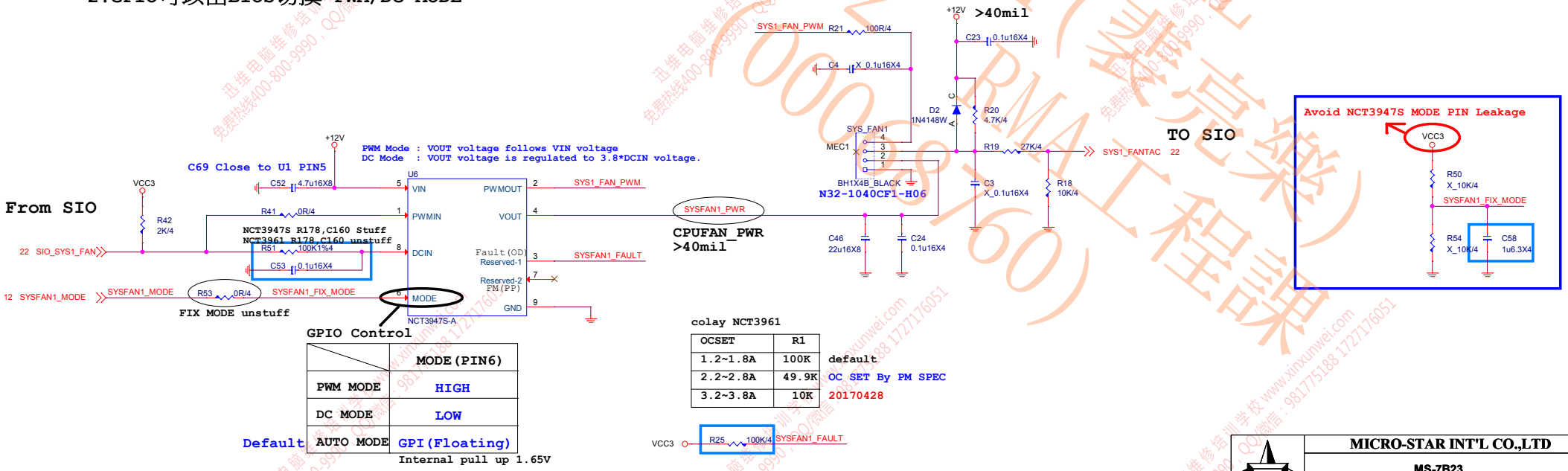
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



MICRO-STAR INT'L CO.,LTD	
MS-7B23	
Size: Custom	Document Description: FAN CONTROLLOR
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RDC(2018041202)
(6000816)
RMA工程策(保密)
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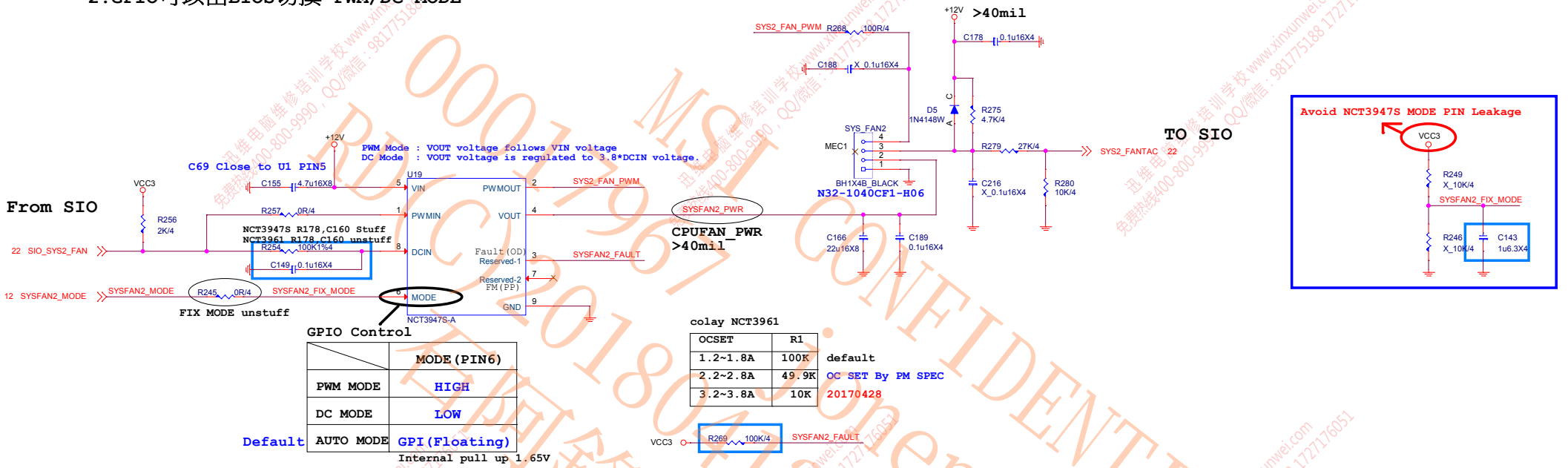
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE

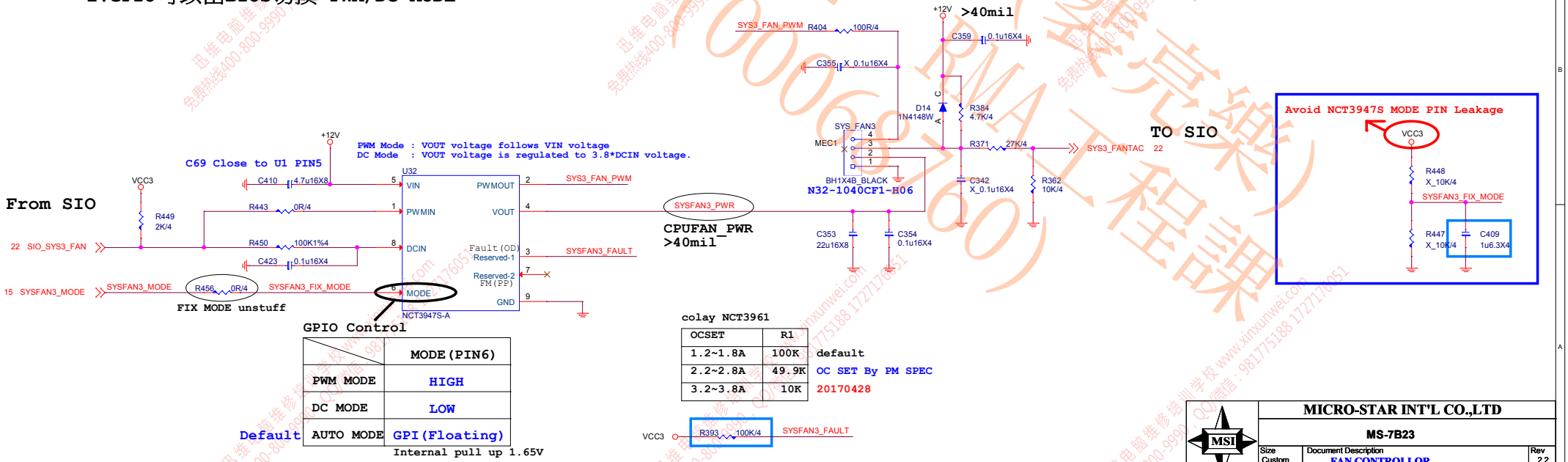


	MODE(PIN6)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



	MODE(PIN6)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

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0001961 MSI CONFIDENTIAL Shenpei(深圳) RMA工程部 RDC20180412 760068760

Type B:
ALC892/887

CA4 closed PIN25
CA3 closed PIN38
CA38 closed PIN38

Closed Pin9

12mA

Closed codec

CA29.CA30 close to Pin27

48mA

Closed Codec

EMI

Closed Codec

dummy loading

0R for cost down

CA52,CA55 close to LA2

SPDIF_OUT

Varistor
D0G-2710510-I05
Close to Jack

2.2k for better recording quality

for rear I/O 6port:
887VD/892:1k

for rear I/O 3port:
887VD/892:75R

Close to Front panel
For HDA/AC97 front cable.

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RUCG0180402702 RMA 1000689760
i-one pei(样品)

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Size: Custom	Document Description: AUDIO - ALC892/887
Rev: 2.2	
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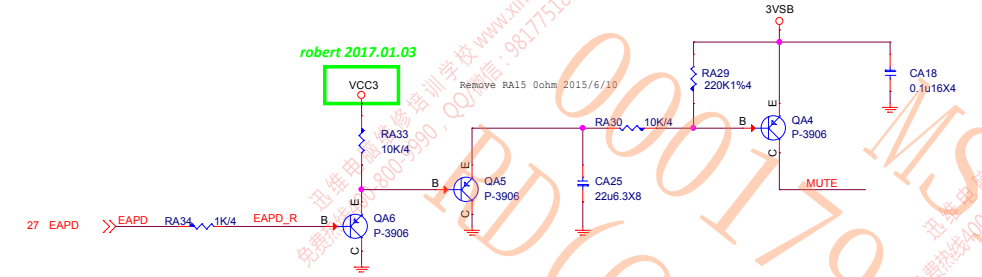
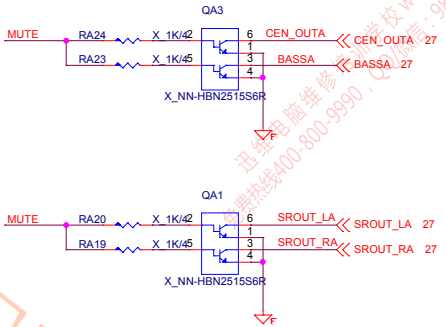
Rear Line OUT De-POP circuit

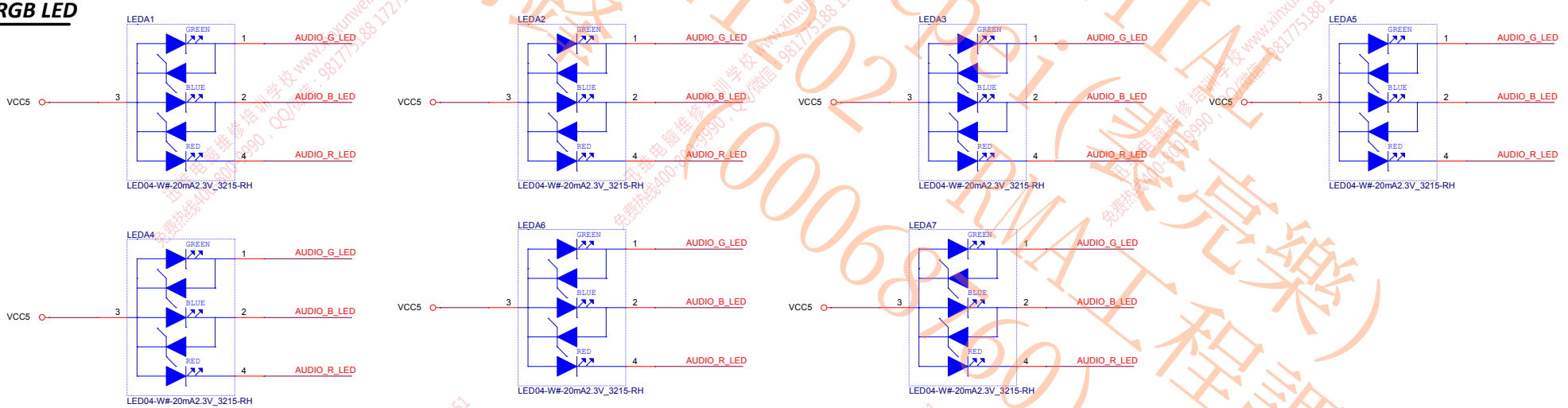
De-pop circuit for Rear Line out & Front Headphone out)

(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA21,CA37, CA38, CA39, CA40, CA41 to TVS)





Audio RGB LED



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MS-7B23

Size	Document Description	Rev
Custom	AUDIO - depop circuit	2.2

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00017967 MSI CONFIDENTIAL jonepei(樊完樂) PD(C)20180412021 RMA工程課 0006820
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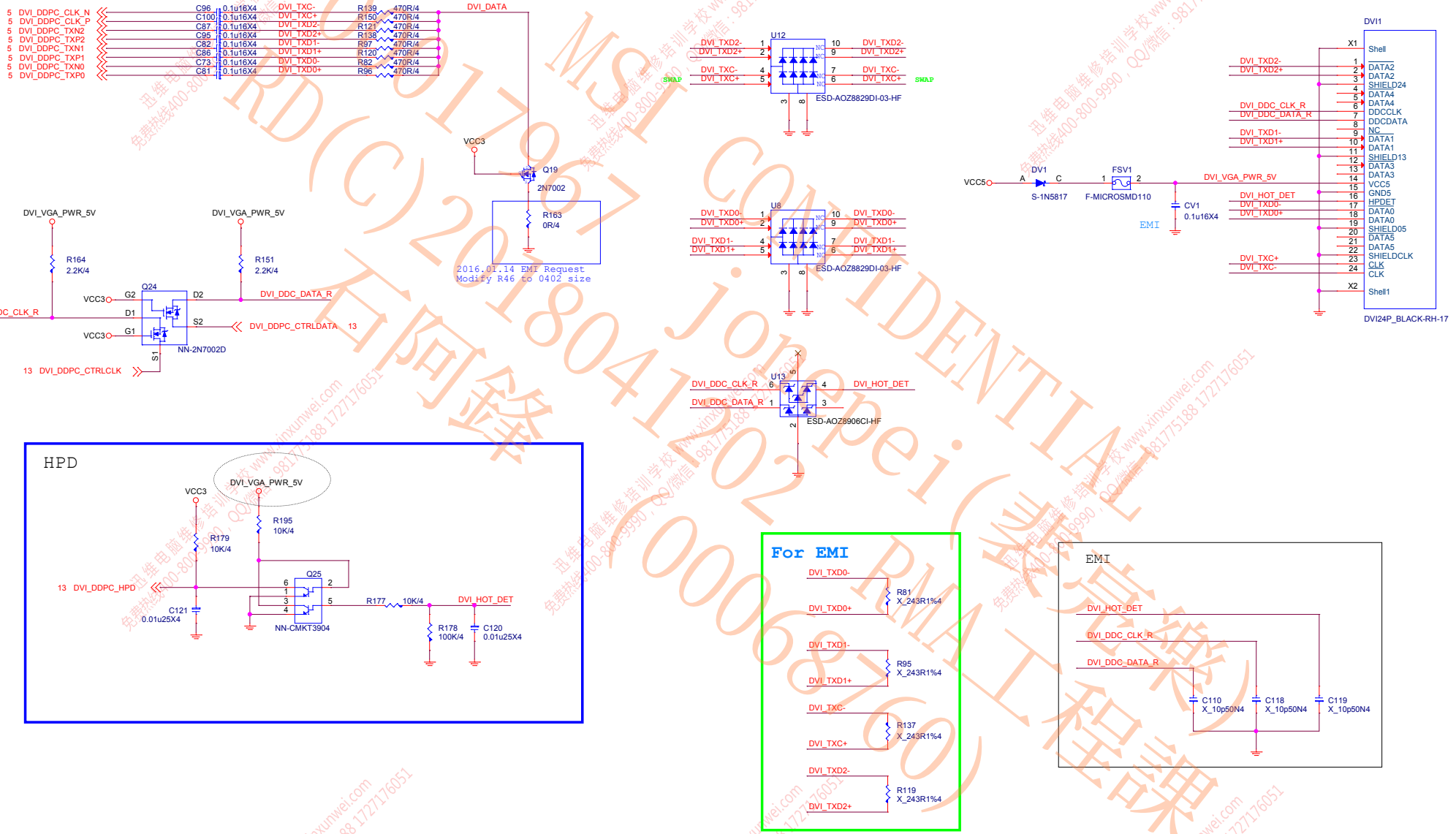
DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



MSI CONFIDENTIAL
jonpei(维修)
RD(C)20180402 RMA工程课
Q01796700068760
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Size: Custom	Document Description: DVI
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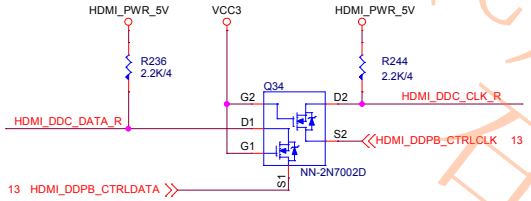
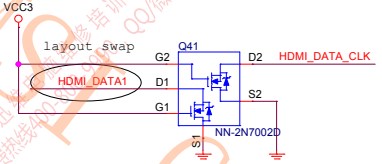
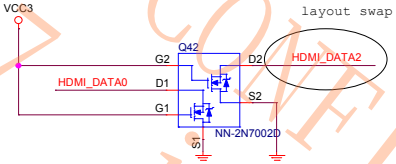
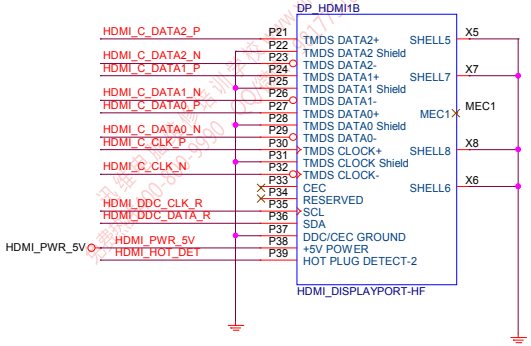
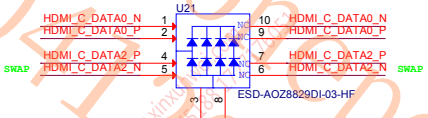
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

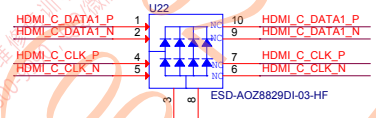


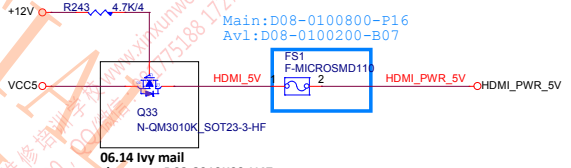




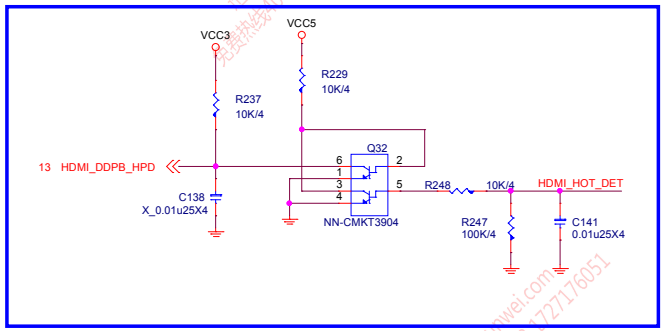


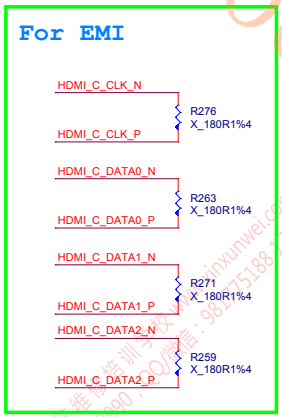


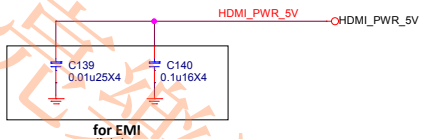


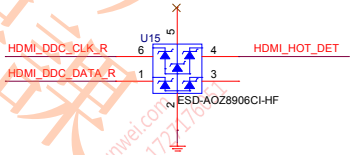


HPD









MICRO-STAR INT'L CO.,LTD

MS-7B23

Size	Document Description	Rev
Custom	HDMI Connector	2.2

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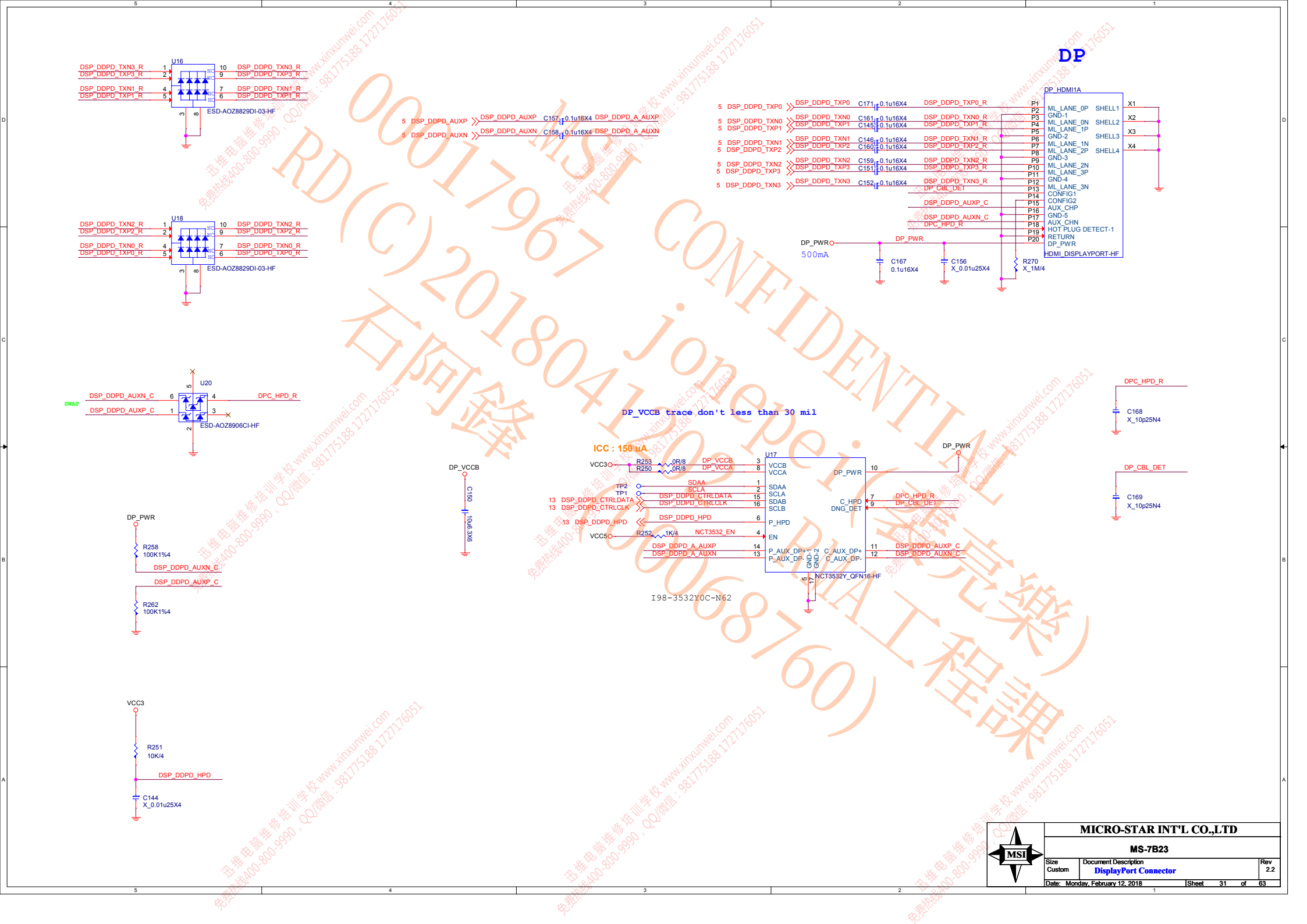
MSI CONFIDENTIAL Jonspei(锦标) RD(C)20180102 RMA工程用 0006876O 石阿锋



MSI CONFIDENTIAL jonepei(樊完荣)
00017967
RD(C)20180412009(BIOS)
PMA工程課
石阿锋
9600068760)
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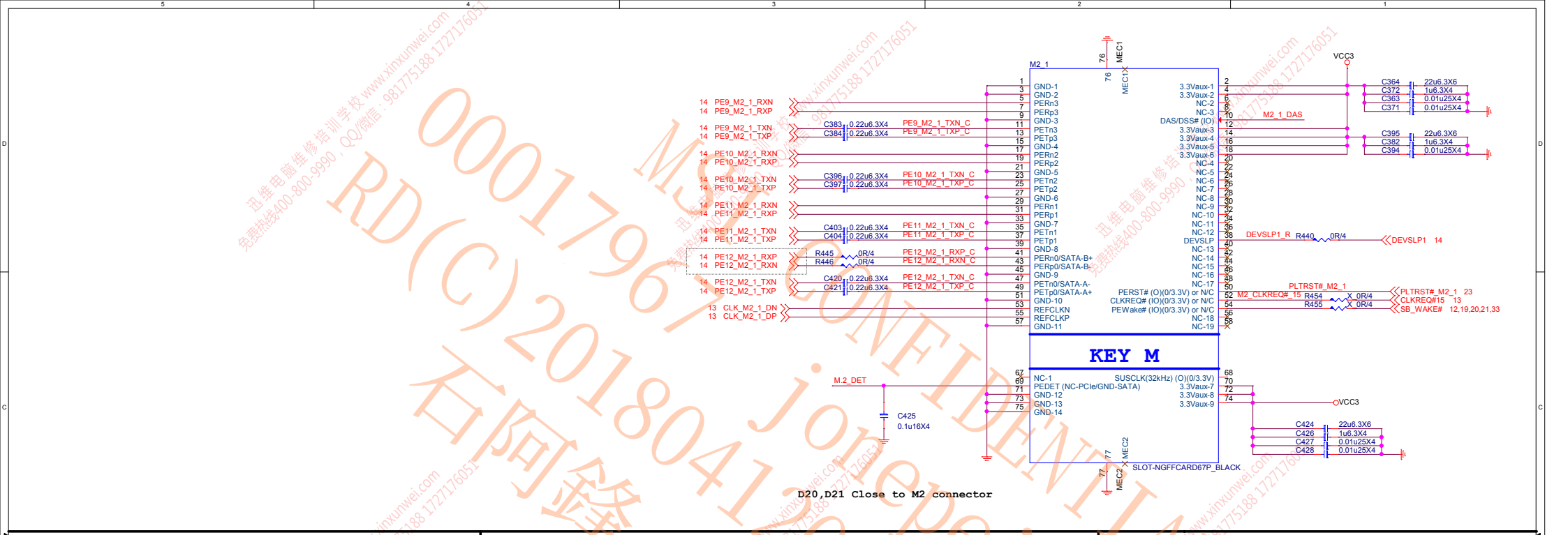
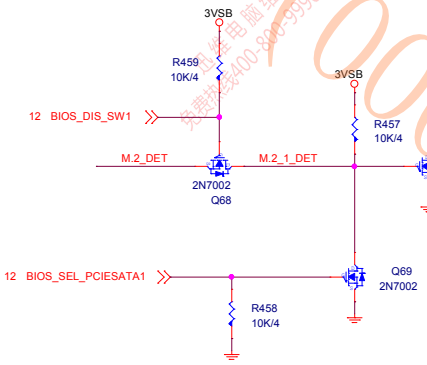
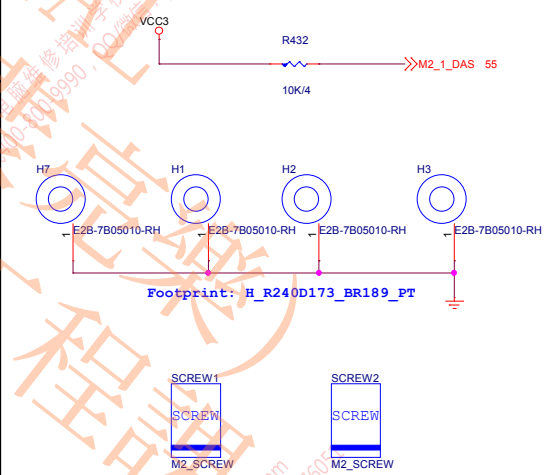


D20,D21 Close to M2 connector



BIOS_MODE

DIS_SW	M1_SEL_PCIESATA	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO



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	MS-7B23	
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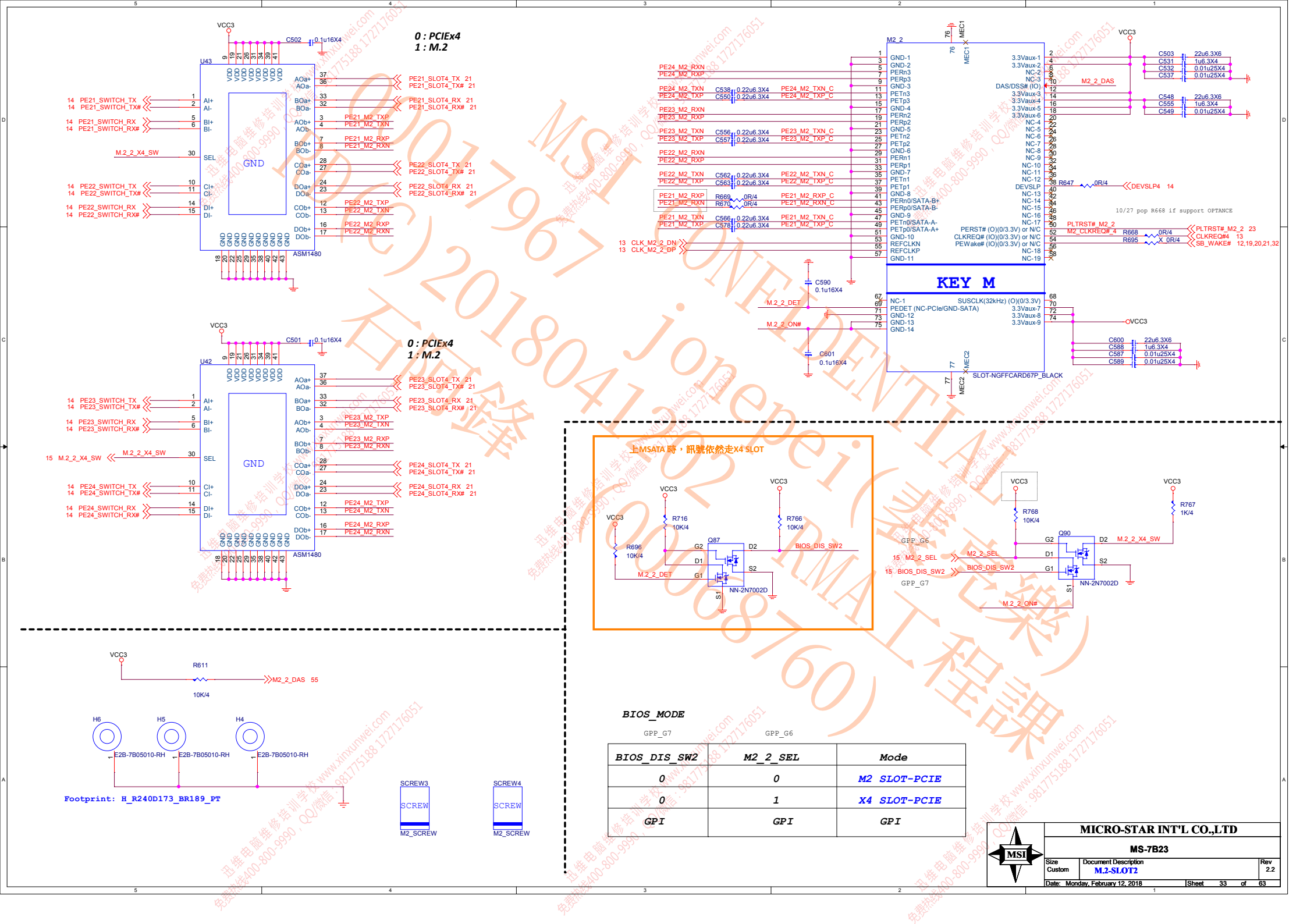
0001796 CONFIDENTIAL
RD(C)20180412 02
RMA工程品
石阿锋（000768760）



BIOS_DIS_SW2	M2_2_SEL	Mode
0	0	M2 SLOT-PCIE
0	1	X4 SLOT-PCIE
GPI	GPI	GPI

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RMA工程師
(0017967 2018041202 60068760)
石晋锋
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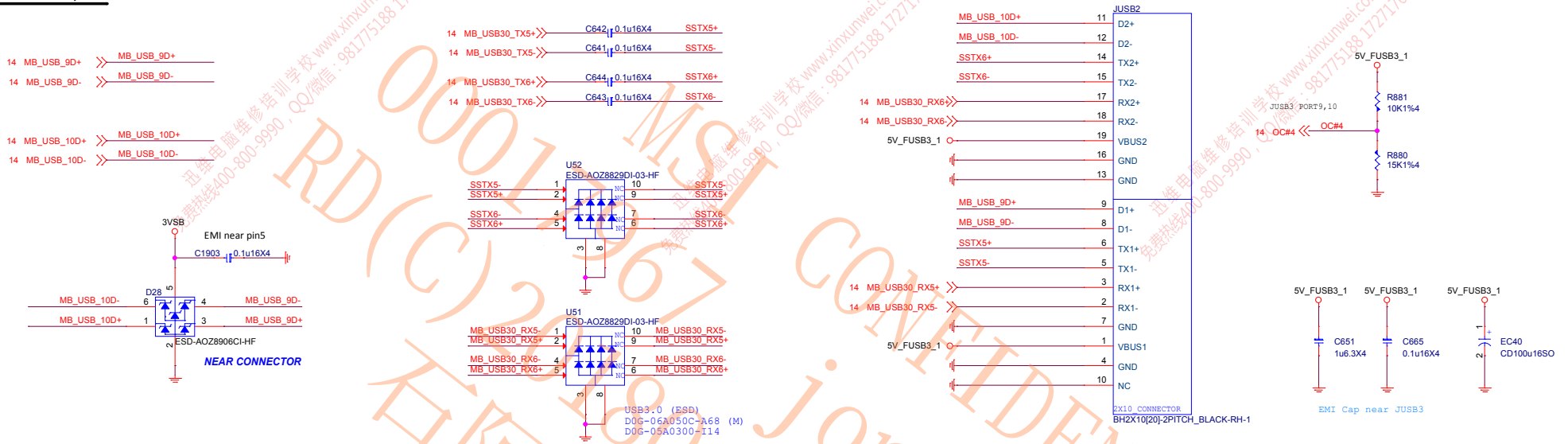
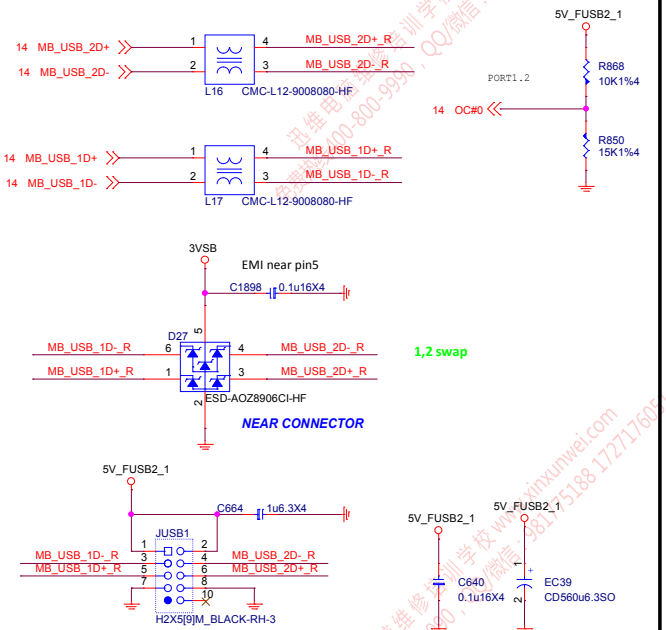
JUSB3 PORT9,10



JUSB1 PORT 7,8

2017.12.12
swap 1,2 to 7,8 for layout



LAN_USB1 PORT 1,2

2017.12.12
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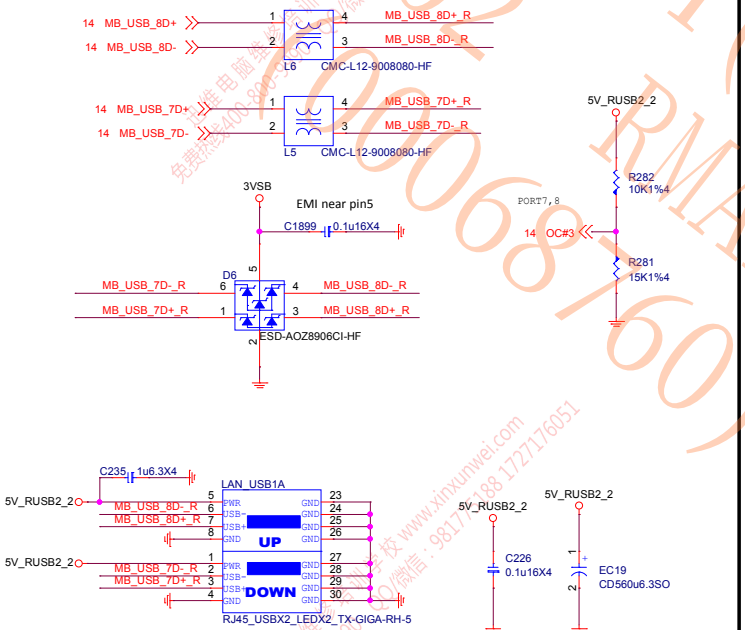
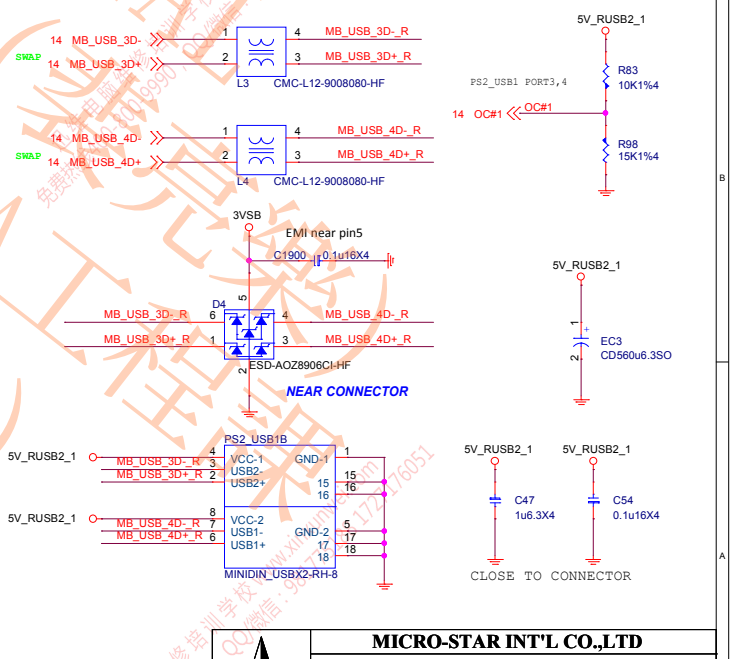


REAR PS2_USB1 PORT 3,4



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Size: Custom	Document Description: Front USB/ PS2_USB1	Rev: 2.2
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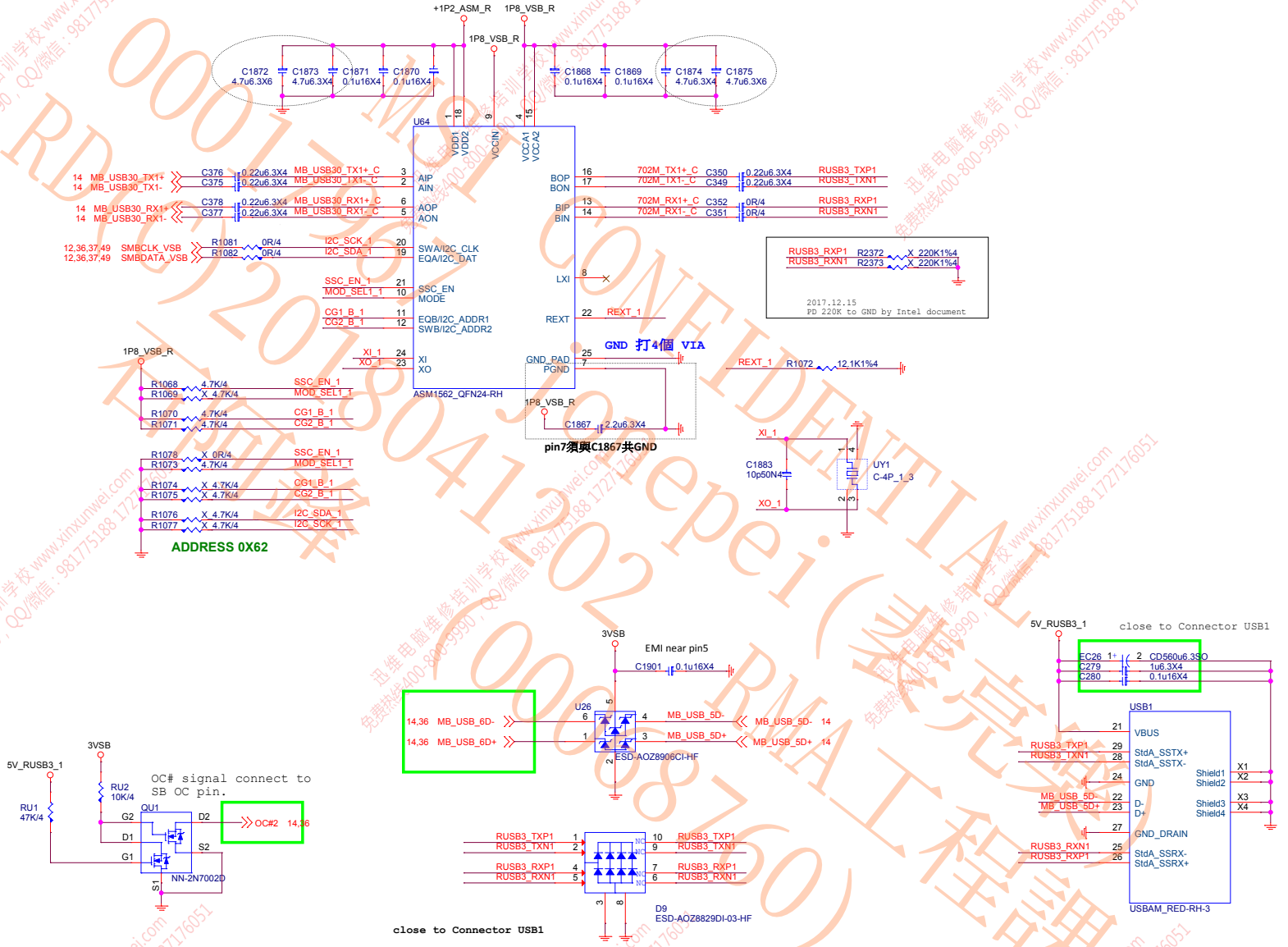
MSI CONFIDENTIAL 0001967 RD(C)2018041202 Jonepc1(0006876O) RMA工程用 石阿修

Rear TYPE-A
USB3.1 Re-Timer



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0001 MSI CONFIDENTIAL Joyepei(樂完美) RD 2018041702 (0068760) RMA工程碟

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MS-7B23	
Size: Custom	Document Description: Type-A & Re_driver
Rev: 2.2	
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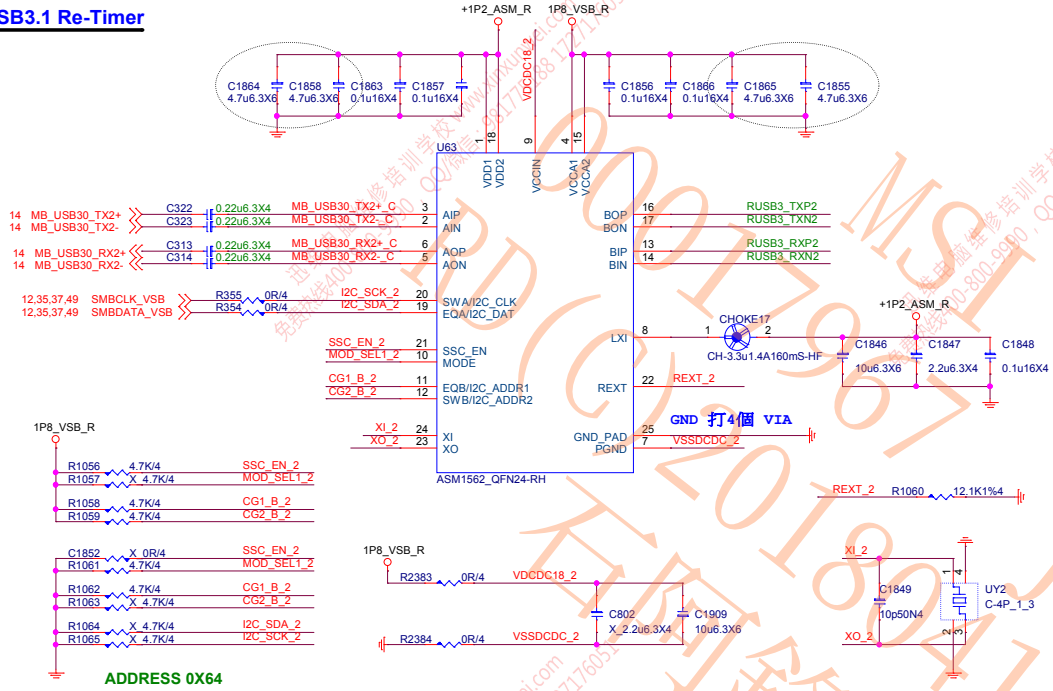
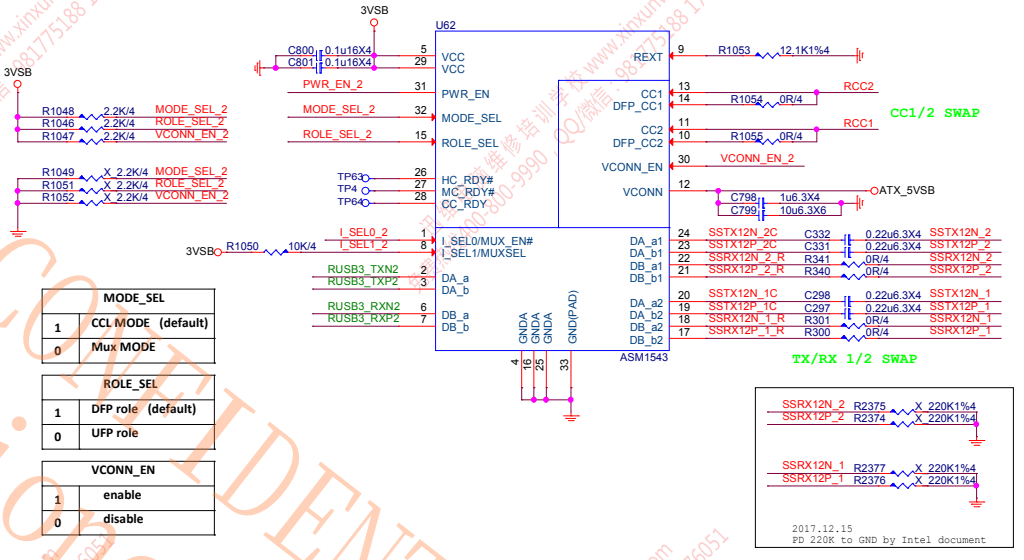
USB3.1 Re-Timer



USB Type-C MUX with Configuration Channel (CC)

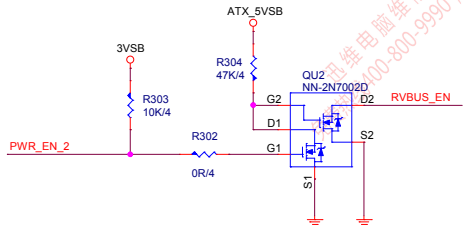


MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

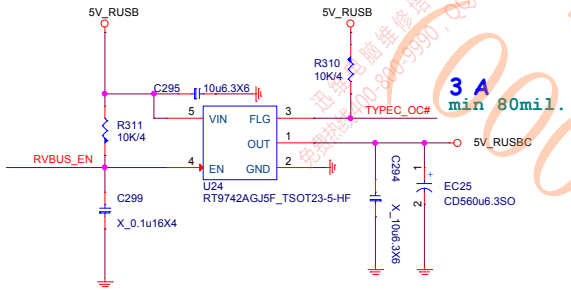
ROLE_SEL	
1	DFP role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable

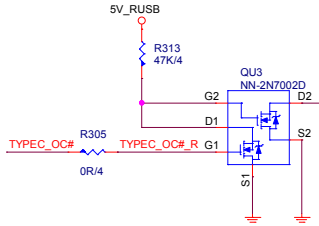
VCOM OC#



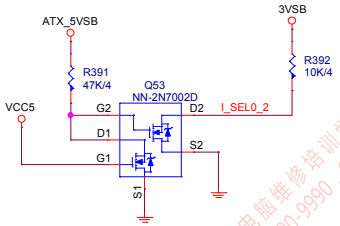
VBUS EN



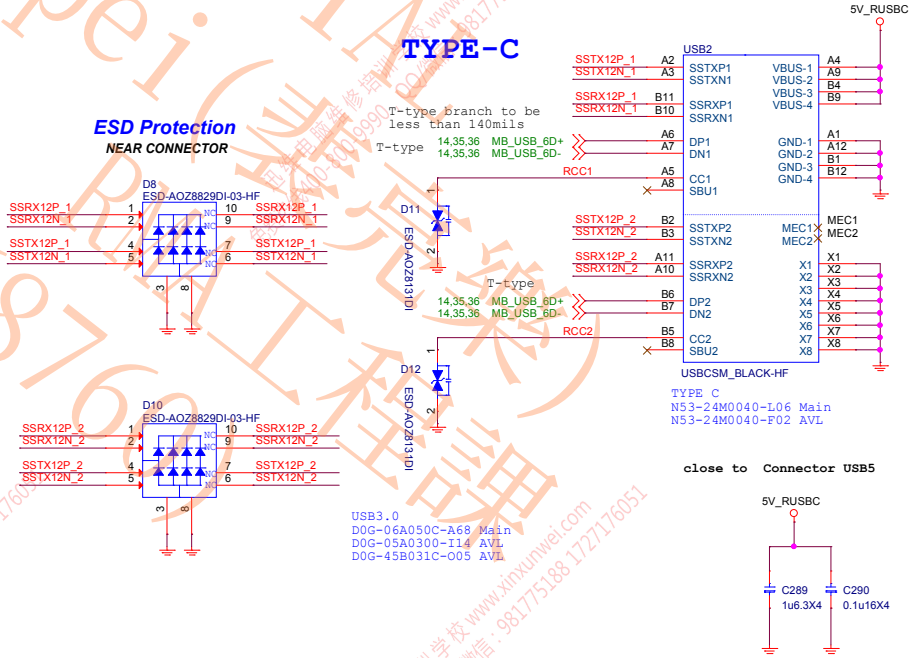
VBUS OC# LEVEL SHIFT



Current Mode



TYPE-C



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2017967 Jinshepei(金社培) 2018412021 RD(C) 6006876 研发(完稿)

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Size: Custom	Document Description: Rear Type-C & Re-Timer
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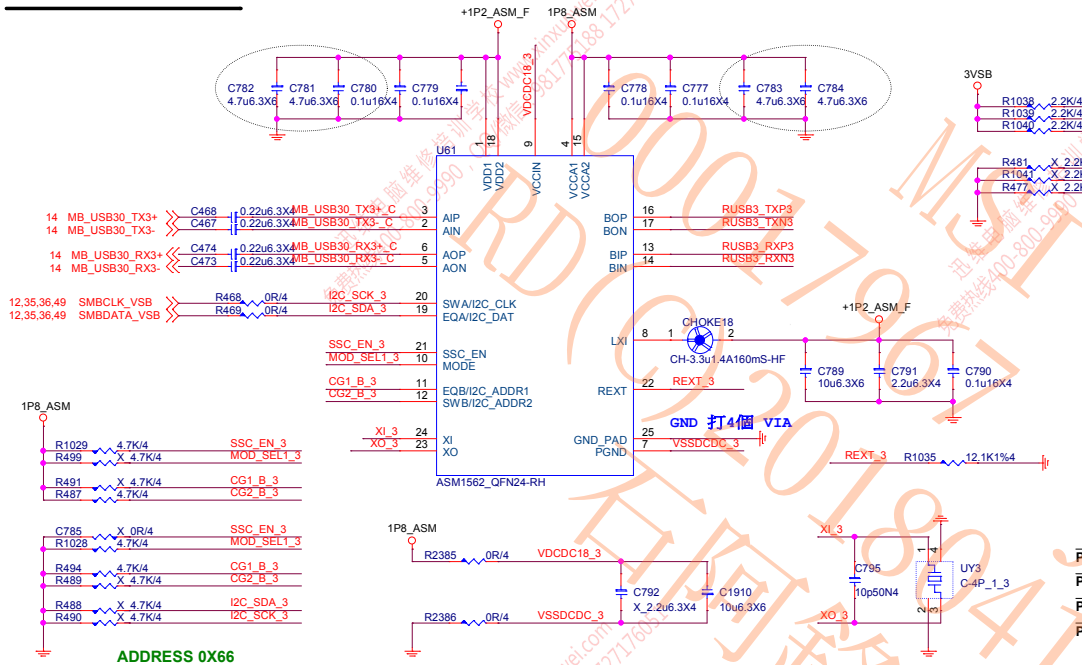
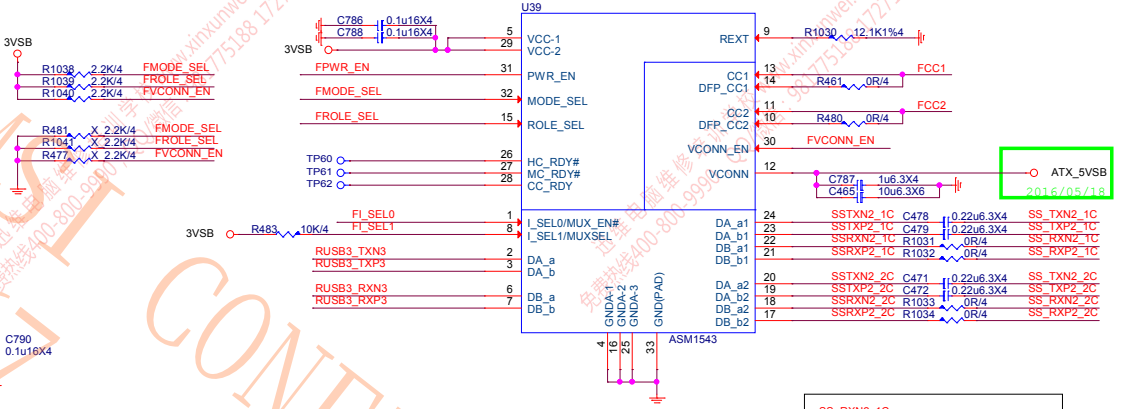
USB3.1 Gen2 Re-Timer

USB Type-C MUX with Configuration Channel (CC)



USB 3.1-Type-C

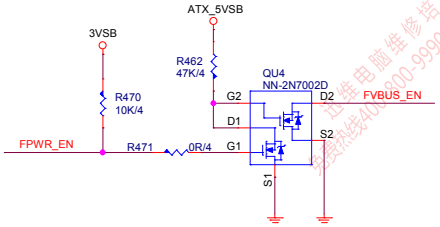


ASM1562 USB3.1 re-timer

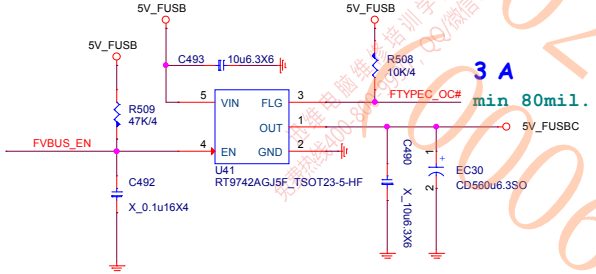
ADDRESS	0x62	0X64	0x66	0x68	0x70	0x72	0x74	0x76	0x78
PIN11 RH (KOhm)	4.7K	4.7K	N/A	4.7K	4.7K	N/A	4.7K	4.7K	N/A
PIN11 RL (KOhm)	N/A	4.7K	4.7K	N/A	4.7K	4.7K	N/A	4.7K	4.7K
PIN12 RH (KOhm)	4.7K	4.7K	4.7K	4.7K	4.7K	4.7K	N/A	N/A	N/A
PIN12 RL (KOhm)	N/A	N/A	N/A	4.7K	4.7K	4.7K	4.7K	4.7K	4.7K

2017.12.15
PD 220K to GND by Intel document

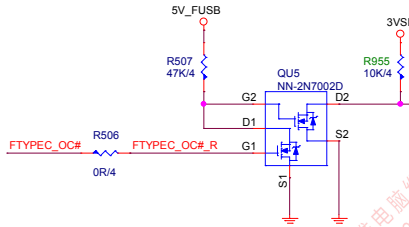
VCOM OC#



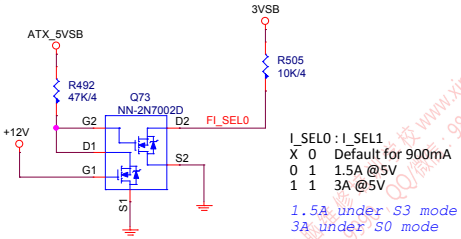
VBUS EN



VBUS OC# LEVEL SHIFT

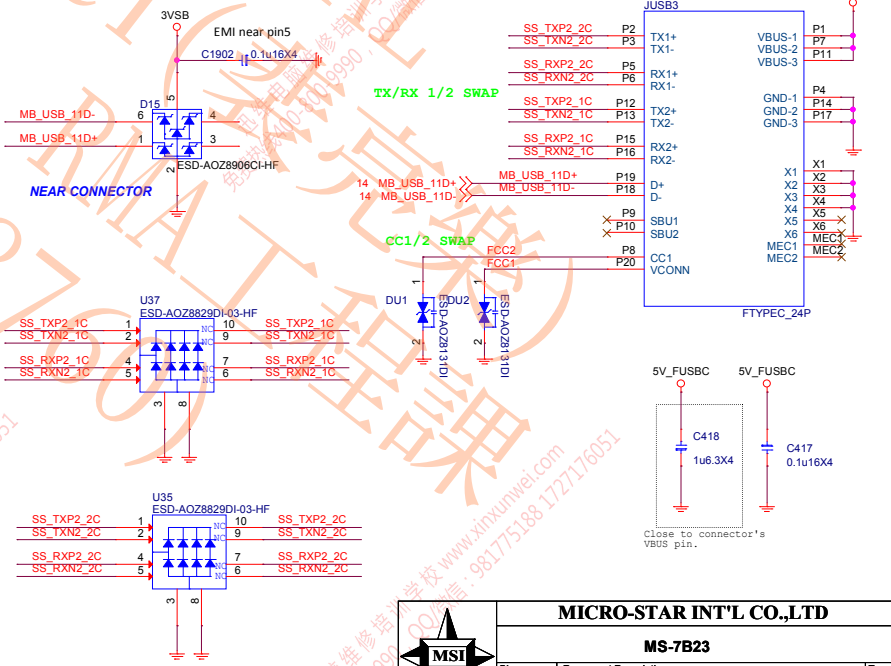


Current Mode



I_SEL0 : I_SEL1
X 0 Default for 900mA
0 1 1.5A @5V
1 1 3A @5V

1.5A under S3 mode
3A under S0 mode



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Size: Custom	Document Description: Front Type-C & Re-driver
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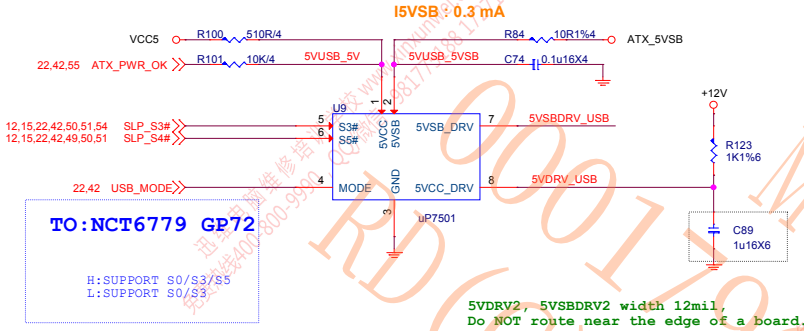
USB POWER

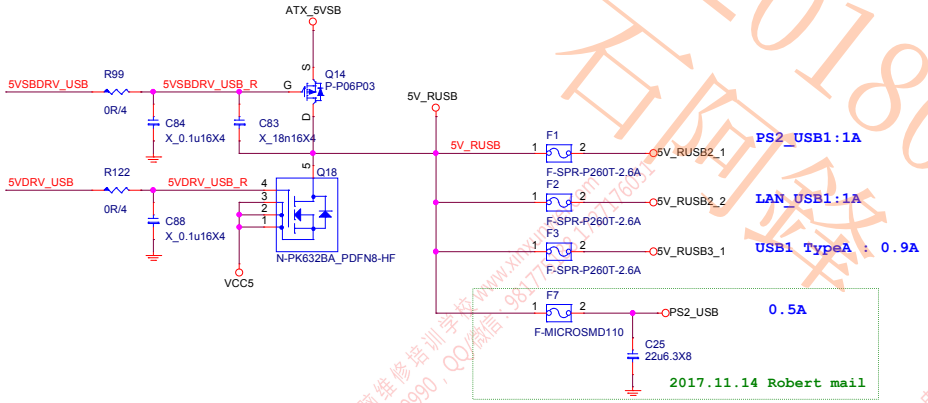


PS2 POWER

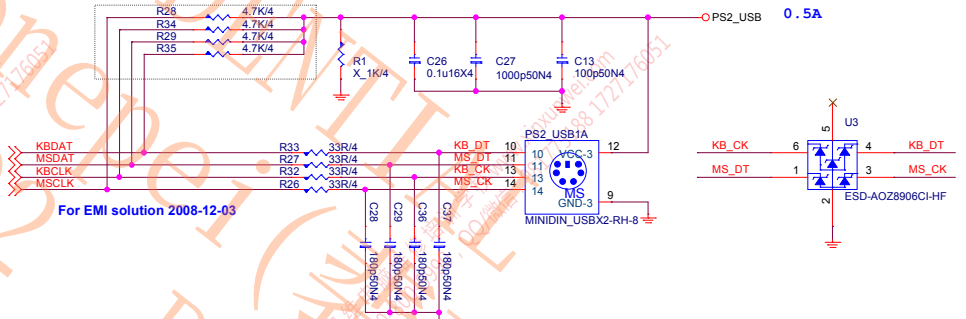
USB MODE

0.5A

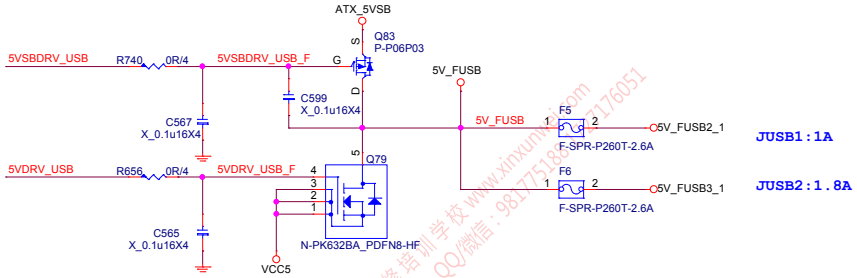
REAR USB PORT POWER



PS2 KEYBOARD & MOUSE CONNECTOR



FRONT USB PORT POWER



USB_CONN	USB_POWER	PCH_PORT	OC# SIGNAL
LAN_USB1	5V_FUSB2_1	Port5,6	OC#0
PS2_USB1	5V_RUSB2_2	Port9,10	OC#1
USB1	5V_RUSB3_1	Port1,2	OC#2
JUSB3	5V_RUSB3_1	Port3,4	OC#3
JUSB2	5V_RUSB2_1	Port7,8	OC#4

MICRO-STAR INT'L CO.,LTD

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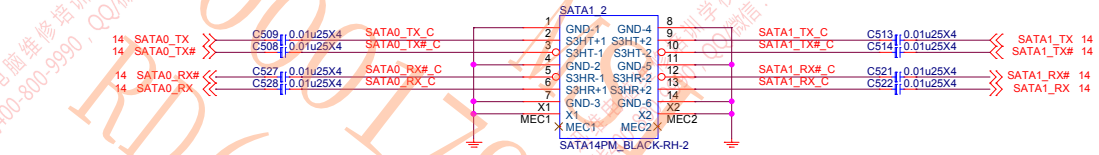
RMA工程課

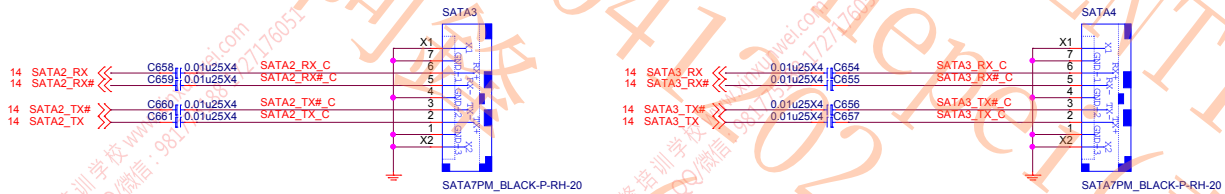
SATA PORT 0,1

Black 90 degree



SATA PORT 2,3

Black 180 degree



00017967 jonesyi CONFIDENTIAL
RD(C)20180412 02
石阿姨(000068760)(装完燊)
RMA工程課
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MICRO-STAR INT'L CO.,LTD		
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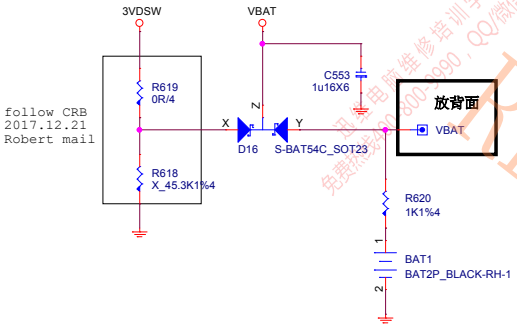
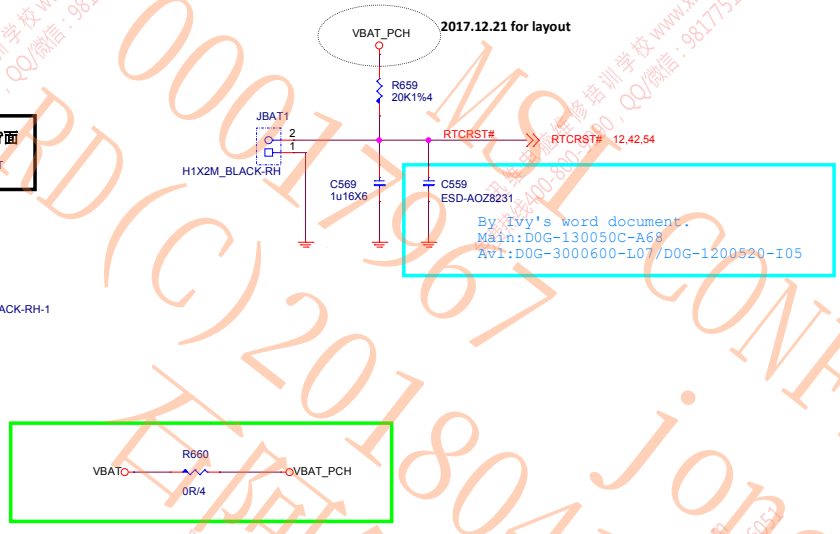
VBAT



Cut VBAT



Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Function 2				
IN		OUT		
INPUT3 & lowswitch_EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default

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Size: Custom	Document Description: CUT VBAT circuit	Rev: 2.2
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MSI CONFIDENTIAL
0001967 jonepei(装完维)
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(0000687160) RMA(下租单)
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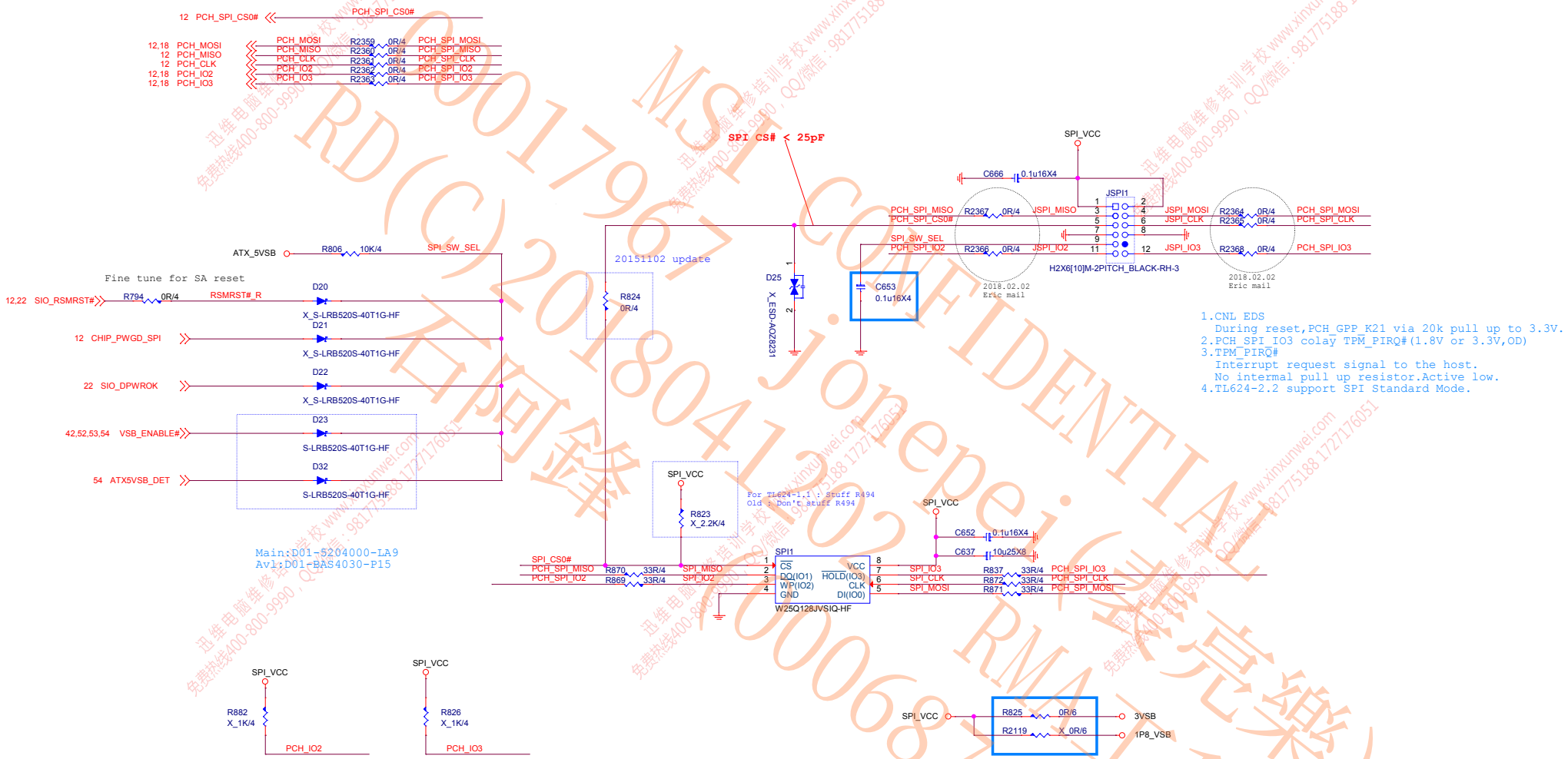

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Size: Custom	Document Description: BIOS ROM	Rev: 2.2
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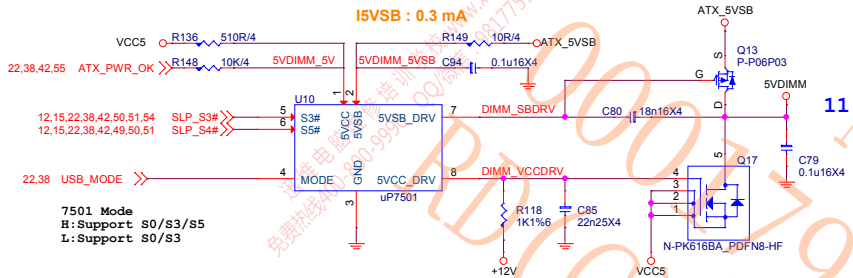
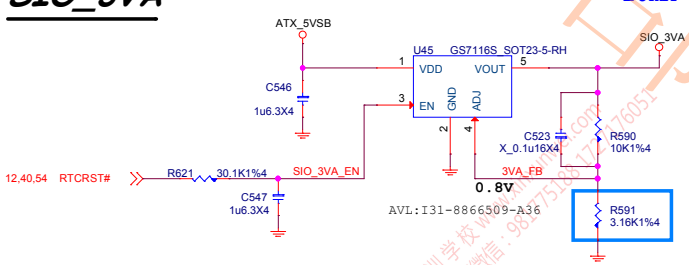
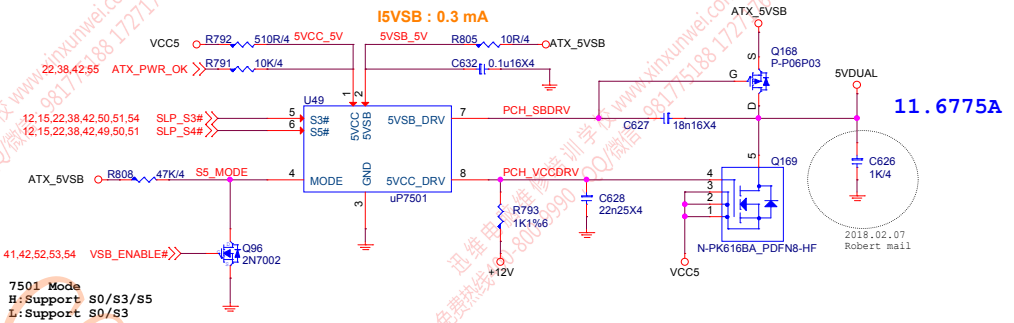
5VDIMM FOR DDR



SIO_3VA

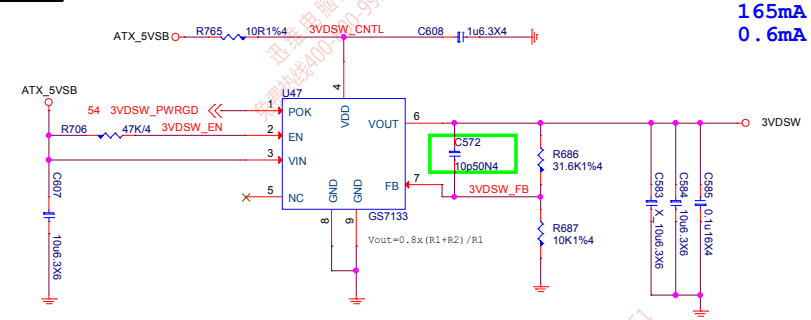


5VDUAL

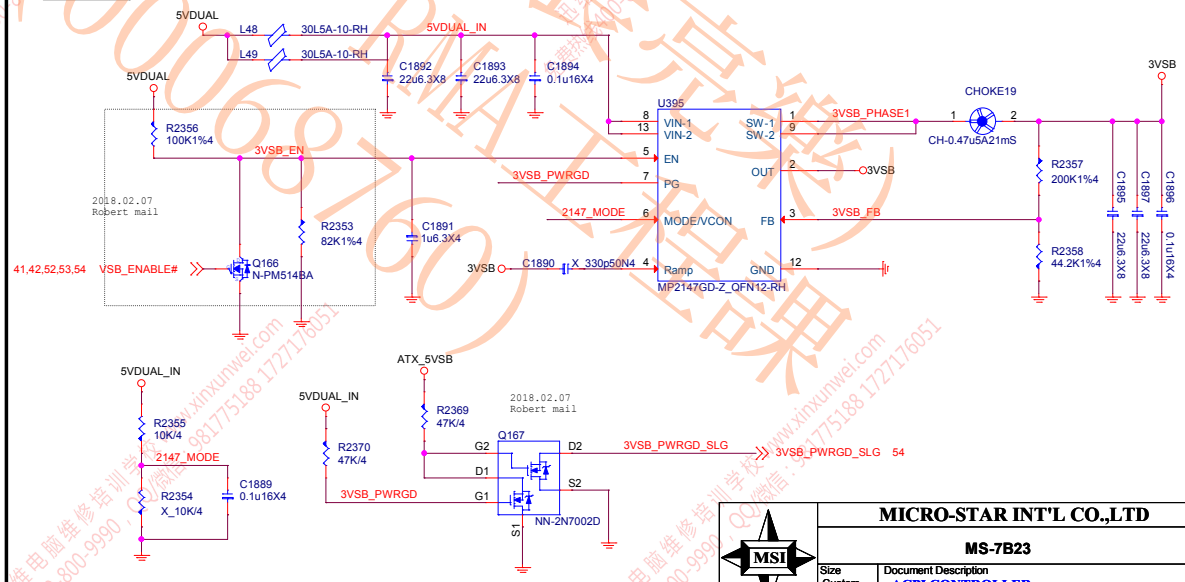


For power 700W solution. (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

3VDSW



3VSB



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MS-7B23	
Size: Custom	Document Description: ACPI CONTROLLER
Rev: 2.2	
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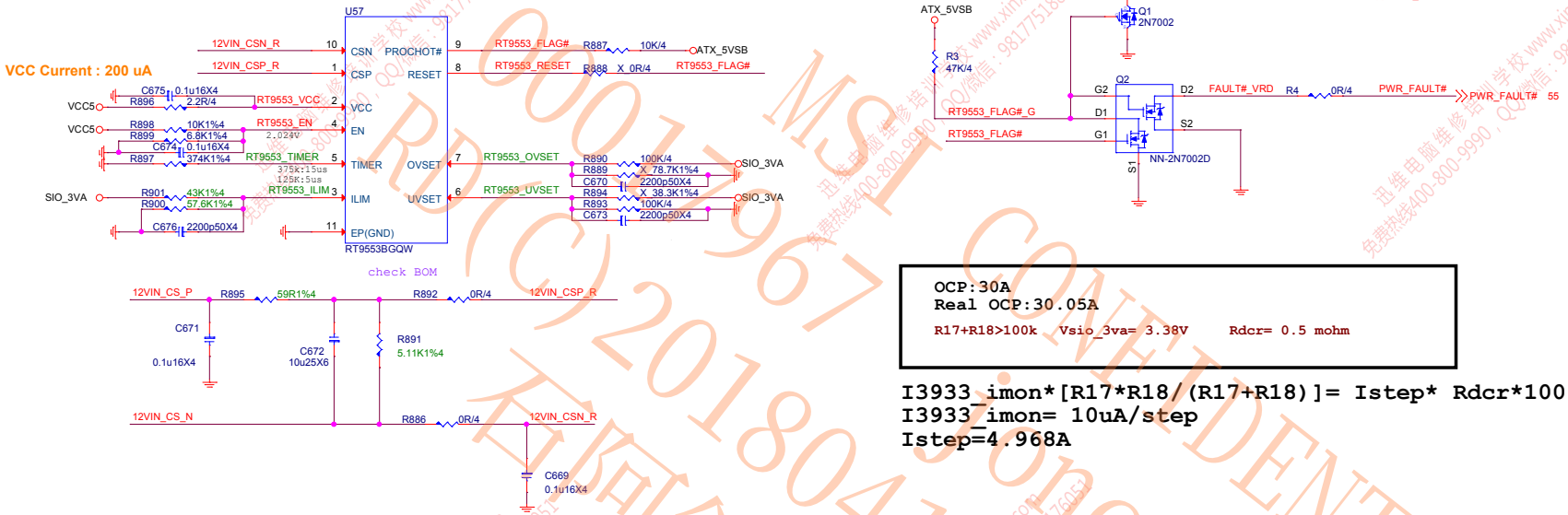
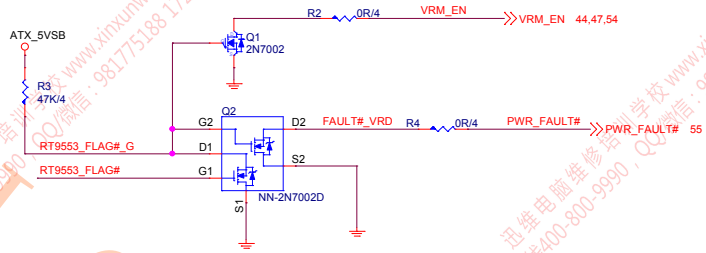
PBA工程部
00017967
PBA(C)20180412028
石阿锋

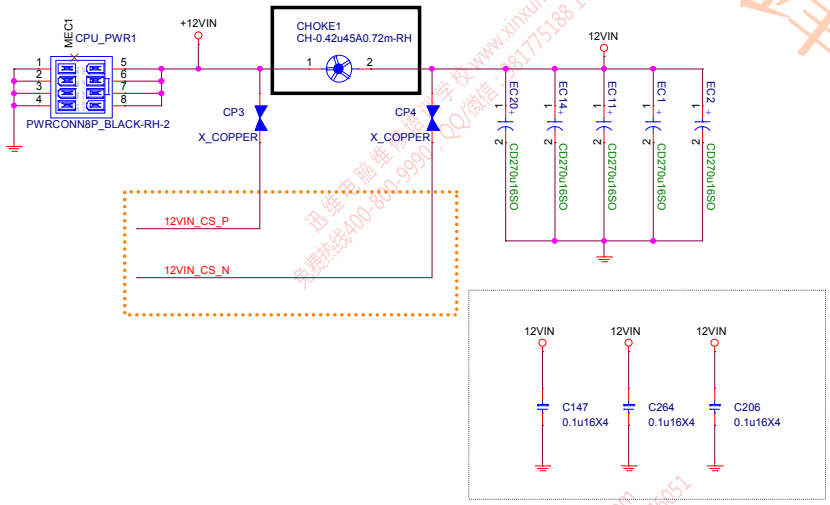




OCP:30A
Real OCP:30.05A
R17+R18>100k Vsio_3va= 3.38V Rdcr= 0.5 mohm

I3933_imon*[R17*R18/(R17+R18)]= Istep* Rdcr*100
I3933_imon= 10uA/step
Istep=4.968A

2017.12.01 Ivy mail
0.22uH->0.42uH



D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.52	> output Vcore
D	=	0.126667	

I o = Icore(max)*0.8			
I core(max)	=	138	> Vcore current
I avg.	=	110.4	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	4	phase
I ripple	=	9.179738	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	2	pcs.

CORE:
D = Vout/Vin
= 1.52/12
= 0.126667
N = 4
Irms = Iout * [D/N - (D)^2]^(1/2)
= 138* (0.031667 - 0.016044)^(1/2)
= 17.2489A

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.52	> output Vcore
D	=	0.126667	

I o = Icore(max)*0.8			
I core(max)	=	45	> Vcore current
I avg.	=	36	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	5.986785	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	2	pcs.

GT:
D = Vout/Vin
= 1.52/12
= 0.126667
N = 2
Irms = Iout * [D/N - (D)^2]^(1/2)
= 45* (0.063333 - 0.016044)^(1/2)
= 9.7857A

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	0.95	> output Vcore
D	=	0.079167	

I o = Icore(max)*0.8			
I core(max)	=	6.4	> Vcore current
I avg.	=	5.12	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	1	phase
I ripple	=	1.382393	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	1	pcs.

VCCIO:
D = Vout/Vin
= 0.95/12
= 0.079167
N = 1
Irms = Iout * [D/N - (D)^2]^(1/2)
= 6.4* (0.079167 - 0.006267)^(1/2)
= 1.728A

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Size: Custom	Document Description: 12VIN/CURRENT SENSE-RT9553	Rev: 2.2
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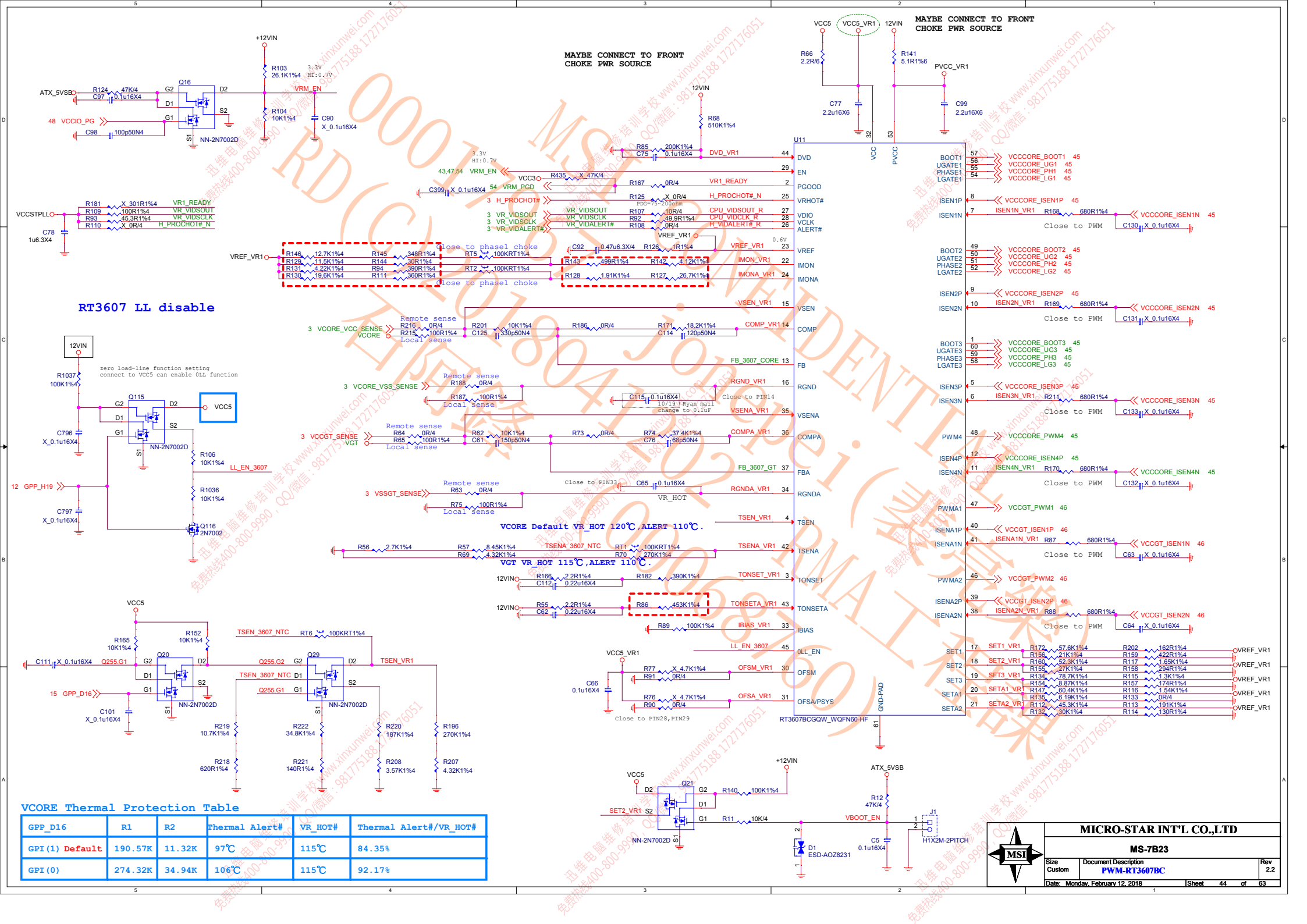
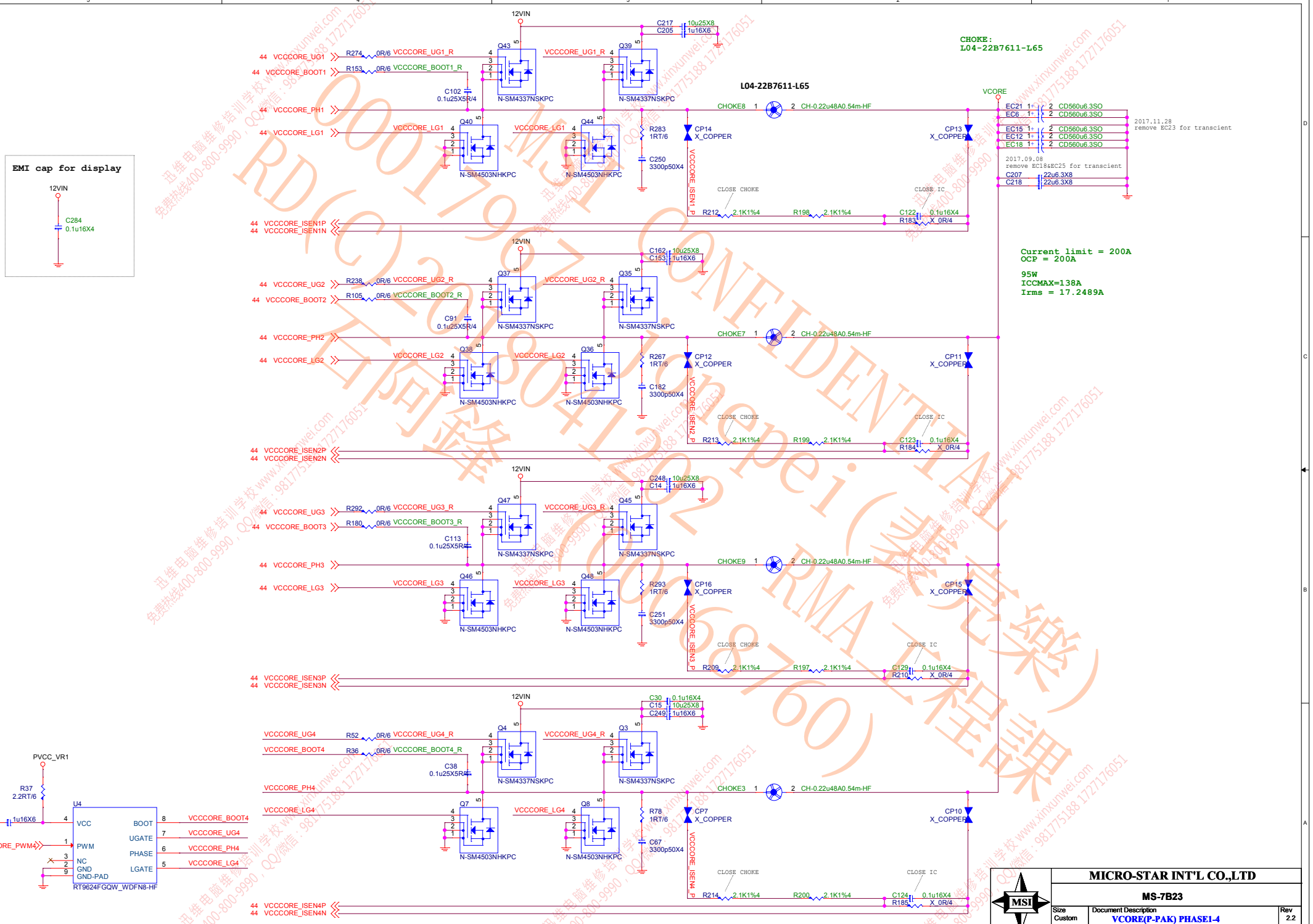
RDC 20180412 V2.0 1000821209 研华科技



VCORE Thermal Protection Table

GPP_D16	R1	R2	Thermal Alert#	VR_HOT#	Thermal Alert#/VR_HOT#
GPI(1) Default	190.57K	11.32K	97℃	115℃	84.35%
GPI(0)	274.32K	34.94K	106℃	115℃	92.17%



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RD(C)2018.04.12 Compal(昆山)
RMA工程課
2006876(760)

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Size: Custom	Document Description: VCORE(P-PAK) PHASE1-4	Rev: 2.2
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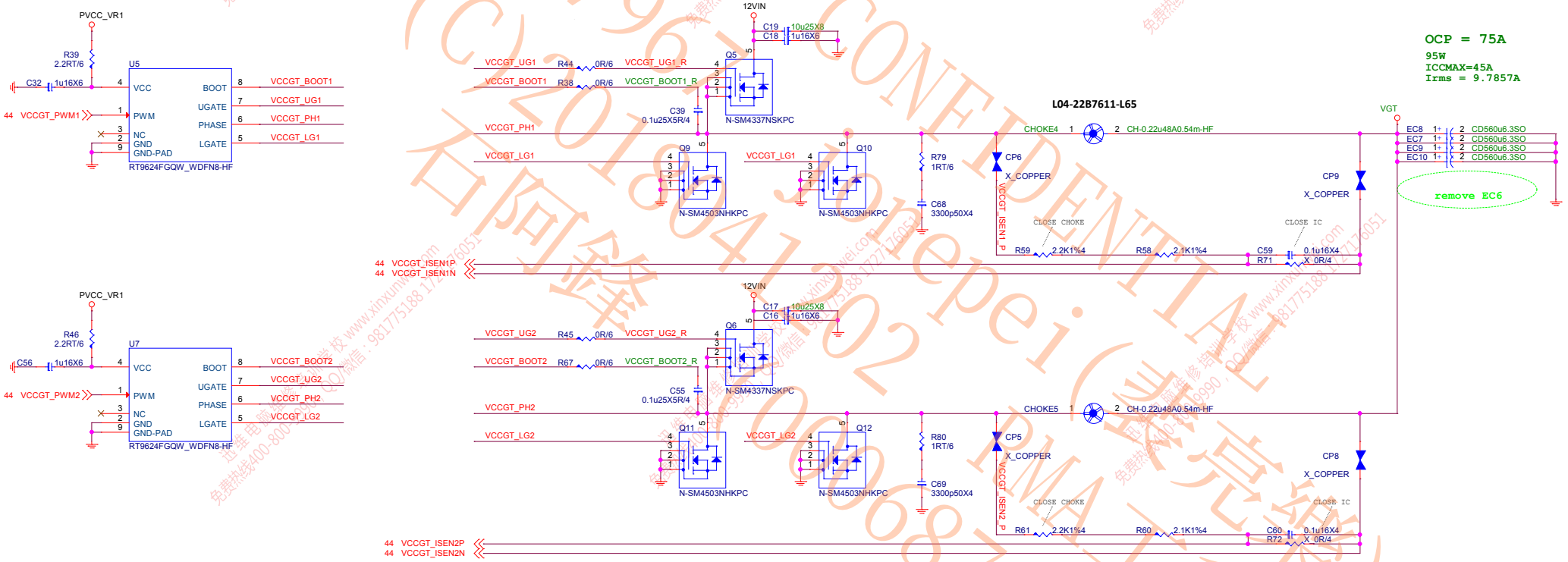

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Size: Custom	Document Description: VGT(P-PAK) PHASE1-2	Rev: 2.2
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MSI CONFIDENTIAL 000179613 Shenpei(审完稿) RD(C)2018041702 PMA工程课 (00068760) 石阿锋

SA Power:1.05V,11.1A

OCP:16.65A

ICC : 1.25 mA

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 16.65* 3mohm / 10uA
= 14.28K

Rdson(low)10V

MOS : 5.1mohm

EN:VIH2.4V
EN pin Maximum:6.5V

FB:0.8V

Vout = Vrefout * (1 + Rpull-up/Rpull-down)
= 0.8 * (1 + 1/3.16)
= 1.053v

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1 * (1.05/12 * (1 - 1.05/12))^(1/2)
= 3.136A

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

2014.08.21 update

Pull up by layout&Check level

EN:VIH2.4V
EN pin Maximum:6.5V

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us

2018.01.31
change to SINOPOWER

snubber

close to L12

0001967 MSI CONFIDENTIAL
RD(C)20180412 02 RMA工程单
石阿锋(0006876)
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Size: Custom	Document Description: VCCSA - POWER RT8125E
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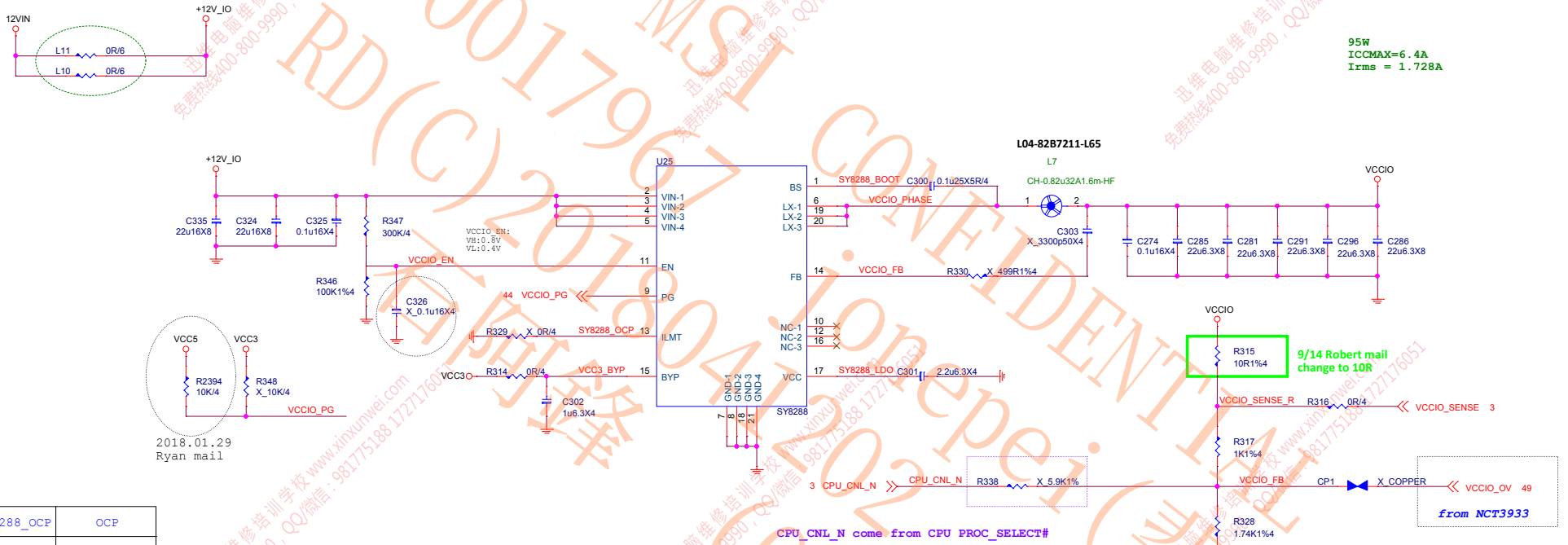
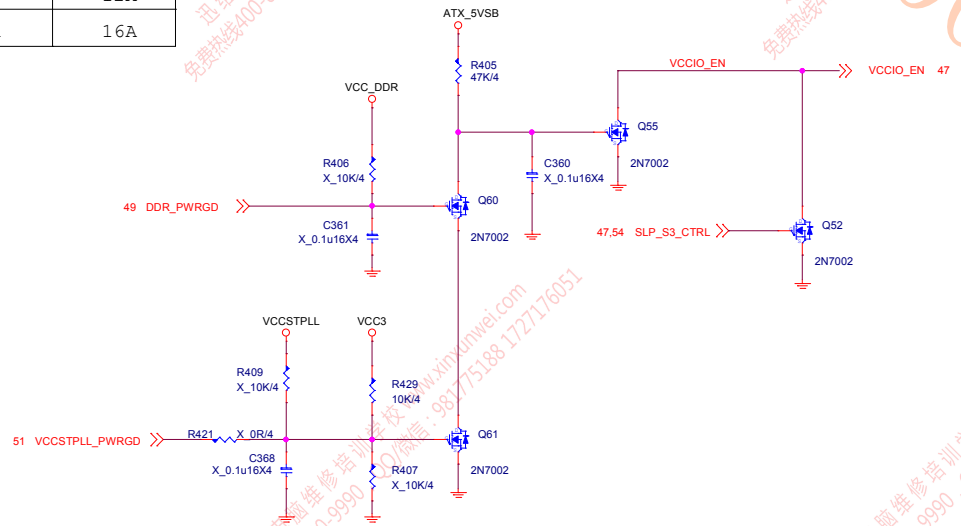
IO Power:0.95V,6.4A

IMAX 10A
ILIMIT=10A~12A
*IOC=ILIMIT+40%*IMAX/2=12A~14A.*



SY8288_OCP	OCP
0	8A
floating	12A
1	16A



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RD(C)20180411202 RMA工程課
(000068760)
0001796 Lonepei(樂完樂)
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MS-7B23	
Size: Custom	Document Description: VCCIO - SY8288
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DDR4 Power:1.2V,19.8A OCP:28A

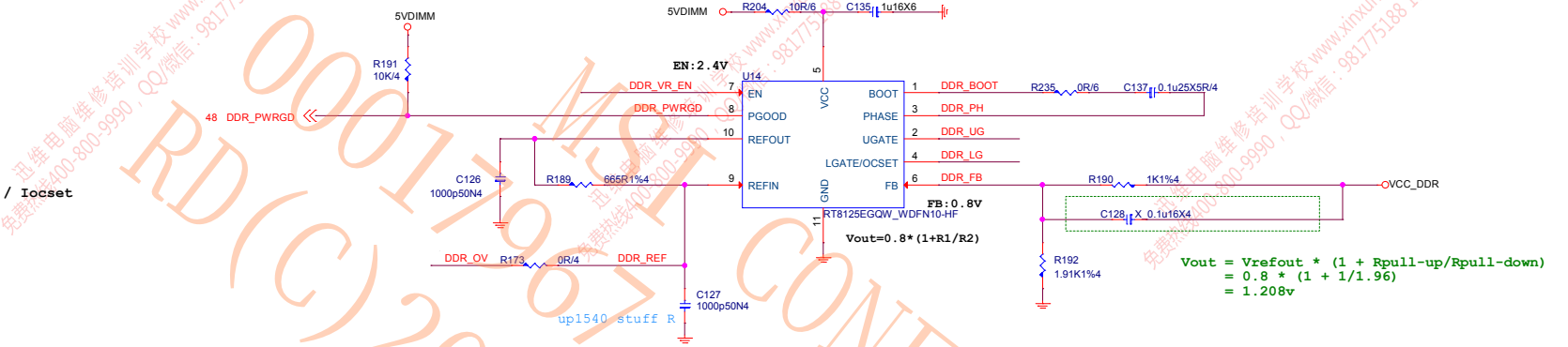
3.3A FOR CPU
15.7A FOR 4DIMM
0.7A FOR DDR VTT

OCP = 19.6A

```
Rocset = 1.5 * Imax * Rdson(low) / Iocset
       = 28* 5.1mohm / 10uA
       = 14.28K
```

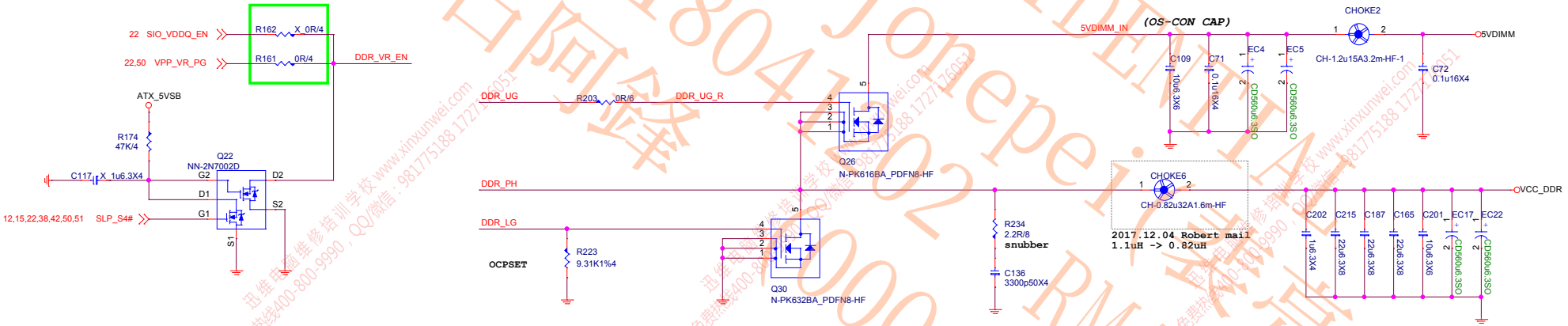
Rdson(low)

D03-4503N0C-ST8 : 5.1mohm



Vout = Vrefout * (1 + Rpull-up/Rpull-down)
= 0.8 * (1 + 1/1.96)
= 1.208v

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 20.2 * (1.2/5 * (1 - 1.2/12))^(1/2)
= 8.627A

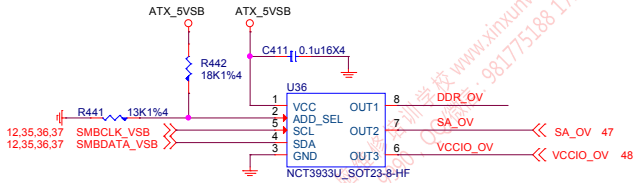


Datasheet公式計算
Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.7677uH (K = 30%)

若帶入CAP ESR計算,0.2432uH＜L＜1.2897uH

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



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Size: Custom | Document Description: DDR - RT8125E | Rev: 2.2

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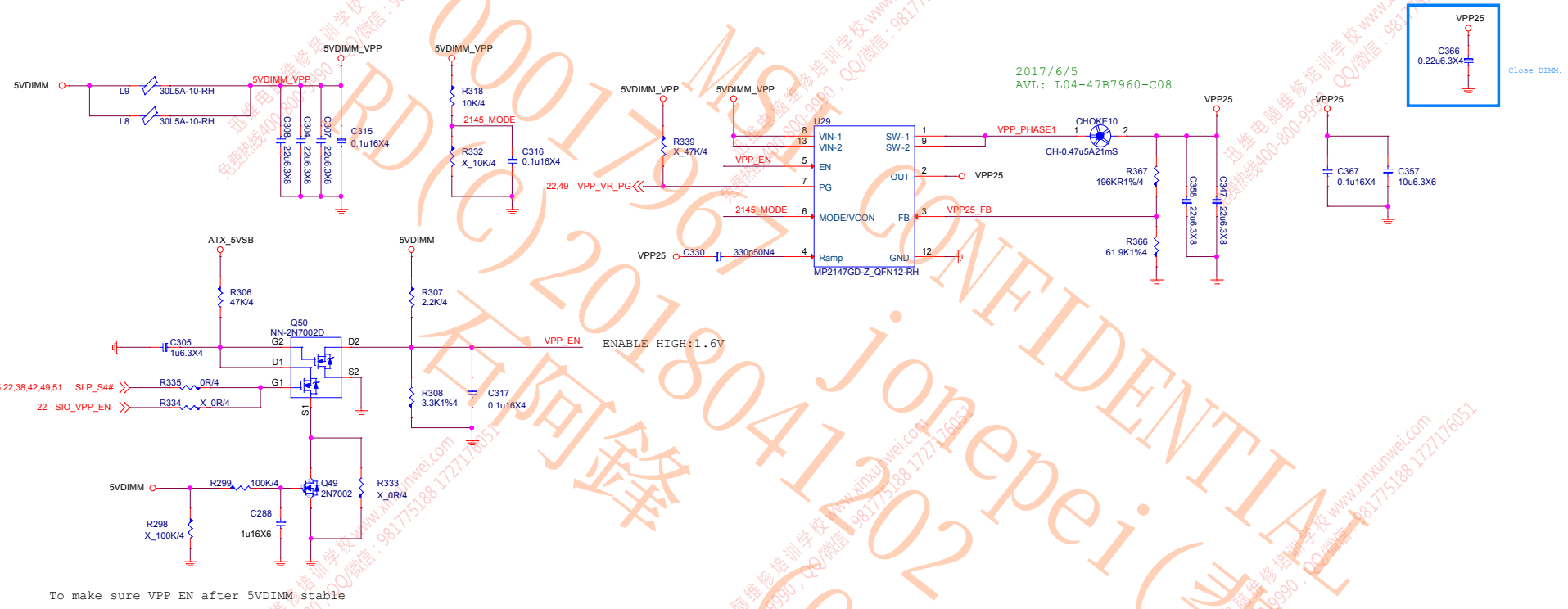
4DIMM :2.24A FOR
DDR VPP2.5V

VPP25 Power

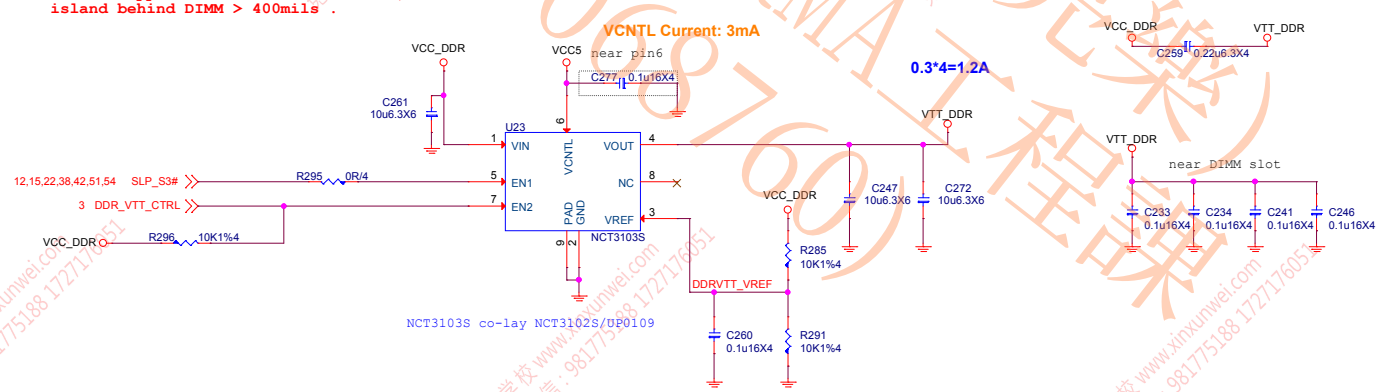
2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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MS-7B23	
Size: Custom	Document Description: VPP-2147 / VTT-3103
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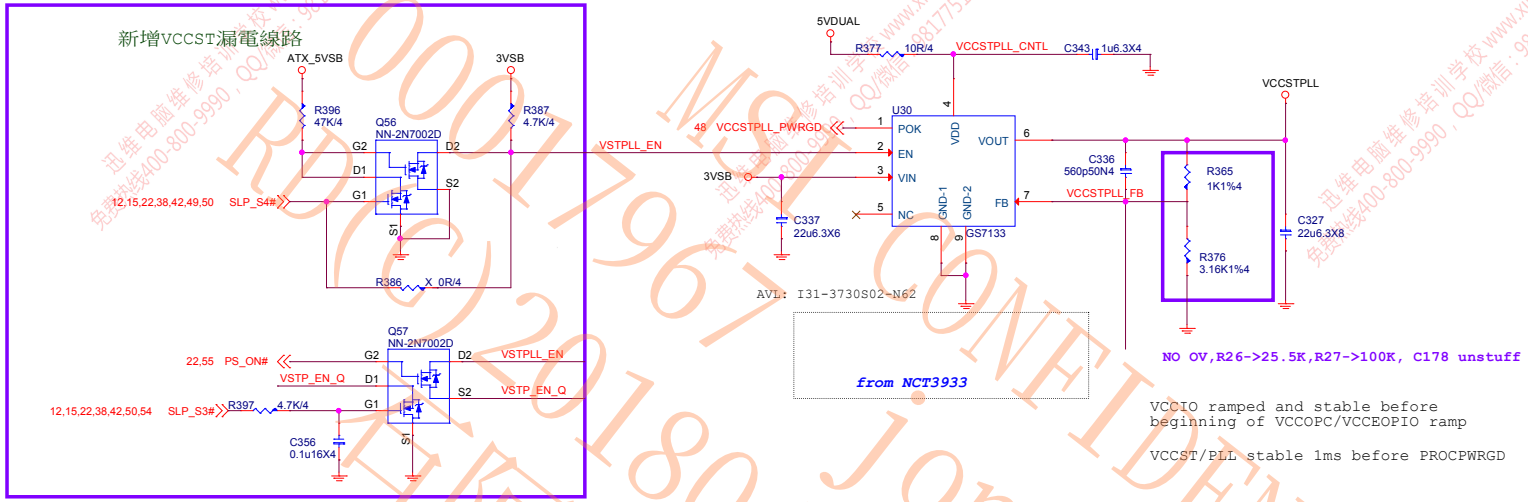
VCCSTPLL

1.05V; 230mA

For Cost down VCCST&VCCPLL merge



NO OV,R26->25.5K,R27->100K, C178 unstuff

VCCIO ramped and stable before
beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

VCCPLL_OC

1.2V; 130mA

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(00068760) RMA工程課

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Size: Custom	Document Description: CPU PWR_ST/PLL_OC	Rev: 2.2
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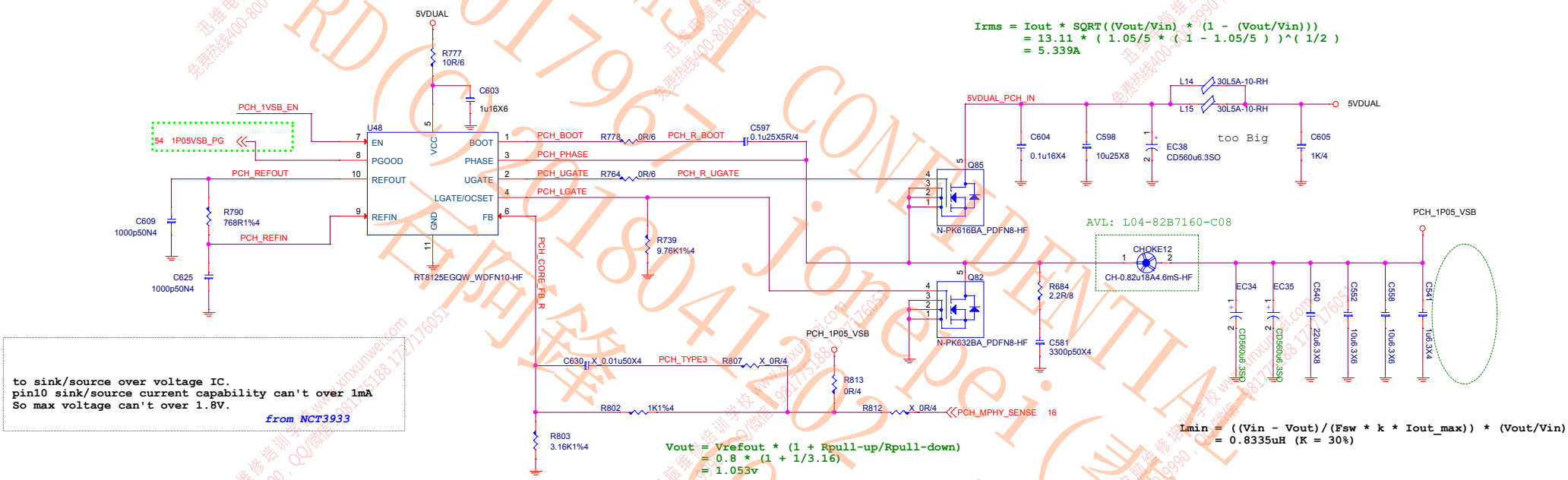
PCH_1VSB

1.05V; 13.1A

OCP=Rocset x Iocset / Rlgds(on)
=9.76K x 10u / 3.3m
= 21.21A

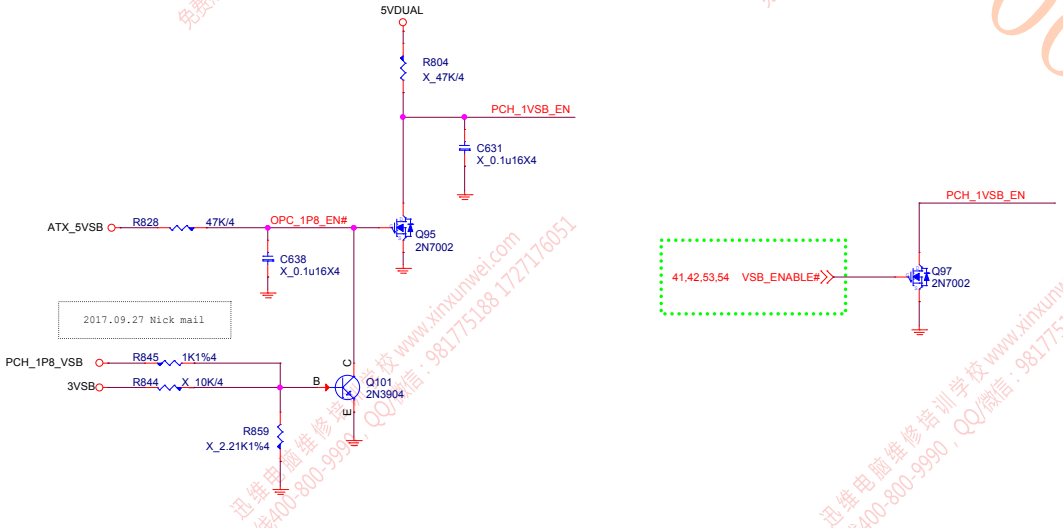


Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 13.11 * (1.05/5 * (1 - 1.05/5))^(1/2)
= 5.339A

to sink/source over voltage IC.
pin10 sink/source current capability can't over 1mA
So max voltage can't over 1.8V.
from NCT3933

Vout = Vrefout * (1 + Rpull-up/Rpull-down)
= 0.8 * (1 + 1/3.16)
= 1.053v

Imin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)



MICRO-STAR INT'L CO.,LTD		
MS-7B23		
Size: Custom	Document Description: PCH Core power	Rev: 2.2
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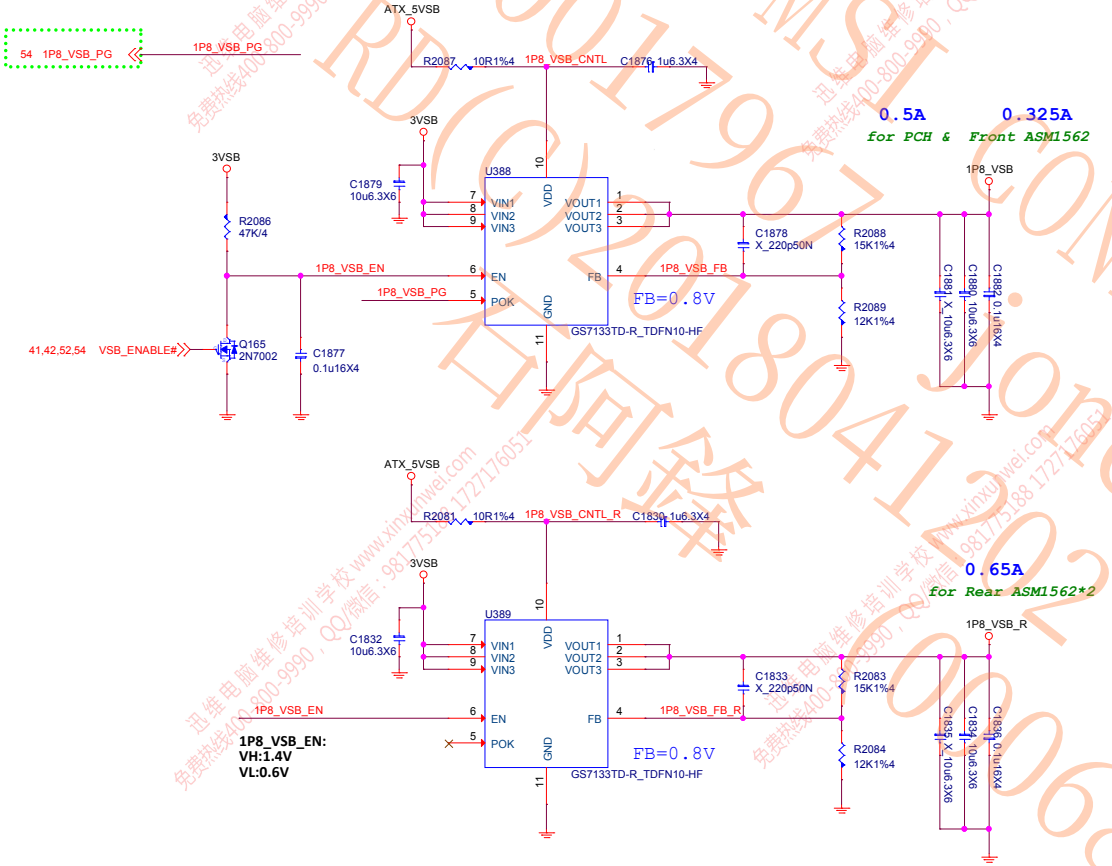
1P8_VSB

1.8V; 500mA

Current Limit: 3.8A

2017.12.07
GS7133 down size to I31-S71330C-N03.



The power consumption with Internal LDO

item	Power state	VCCA 1.8V (mA)	Total power (mW)
Without device plug in,	Power on	25.82	46.47
USB3.1 Gen2 device is plugged in	Burning state	324.60	584.29
USB3.1 Gen2 device is plugged in	In idle	50.58	91.05
USB3.1 Gen2 device is plugged in	S3(D3) state	50.59	91.06

The power consumption with External LDO

item	Power state	VCCA 1.8V (mA)	VDD 1.2V (mA)	Total power (mW)
Without device plug in,	Power on	10.46	17.47	39.79
USB3.1 Gen2 device is plugged in	Burning state	95.34	226.37	443.25
USB3.1 Gen2 device is plugged in	In idle	17.18	52.10	93.44
USB3.1 Gen2 device is plugged in	S3(D3) state	17.17	52.10	93.42

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Size	Document Description	Rev
Custom	PCH 1P8V	2.2

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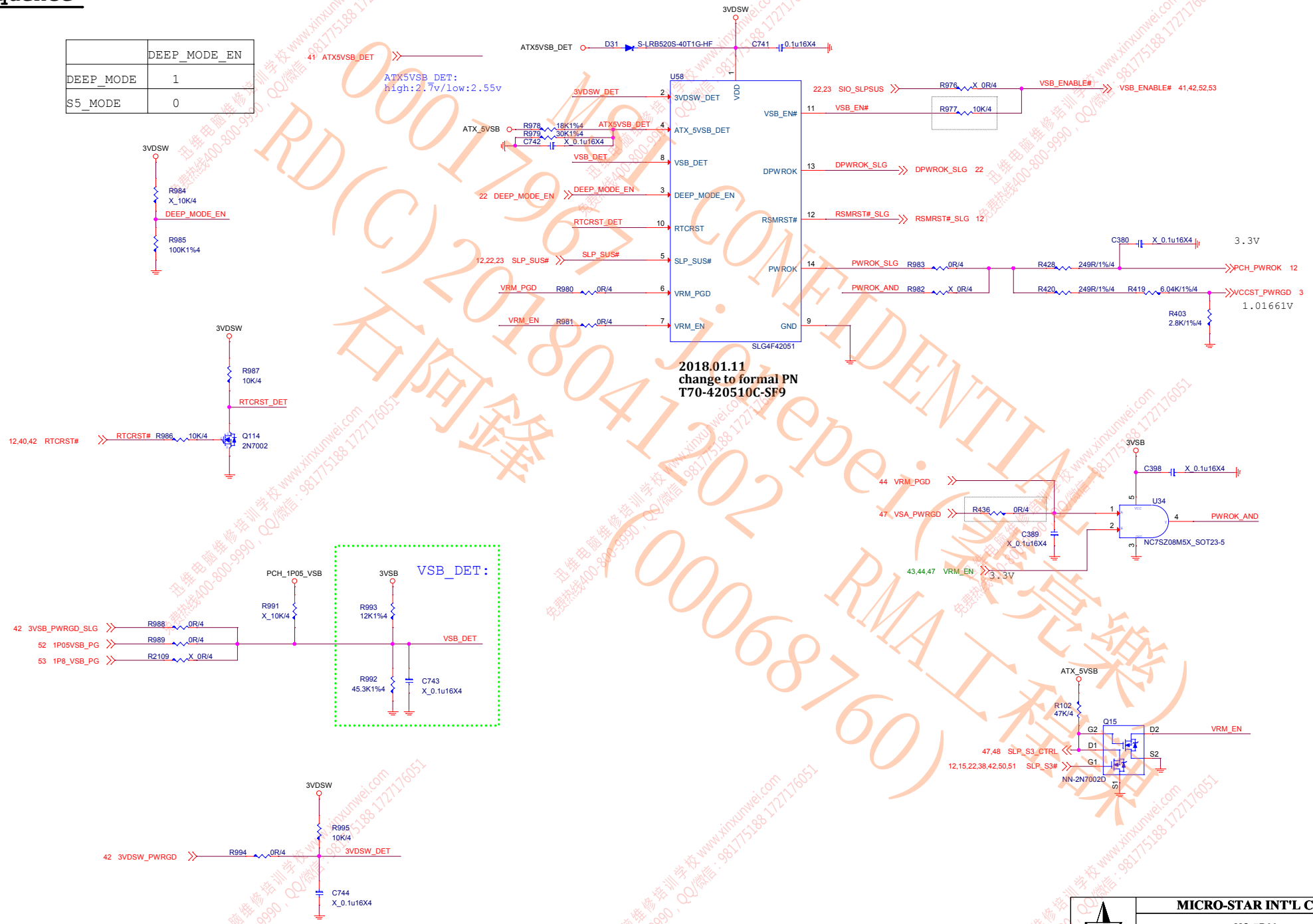
Sequence

	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0



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RD(C)20180412 Jiepei(接受维)
石阿锋 (00068760) RMA工程师

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MS-7B23

Size	Document Description	Rev
Custom	CPU PWR-VRM-Seqence	2.2

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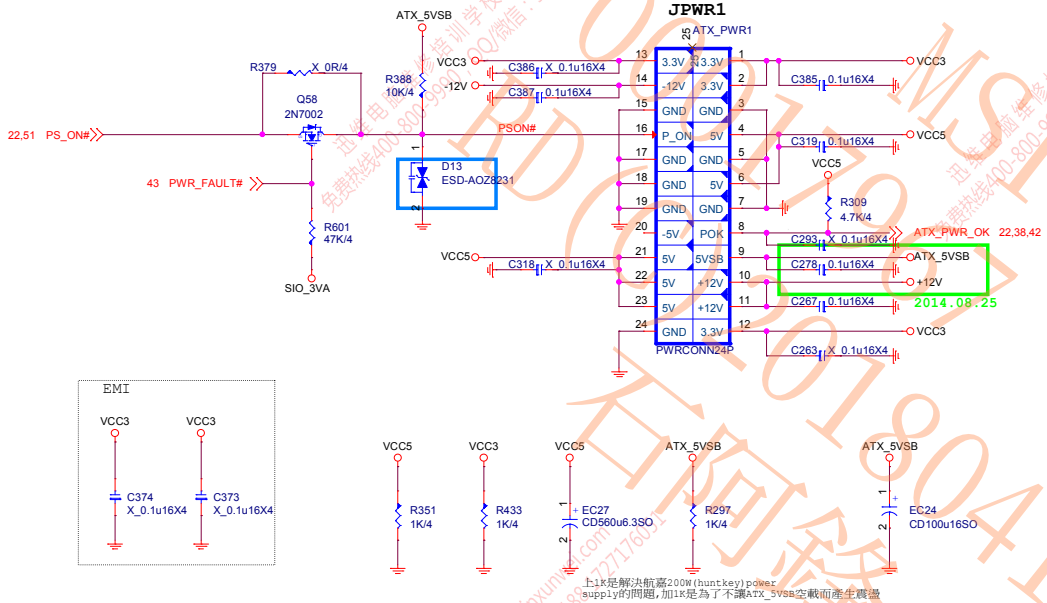
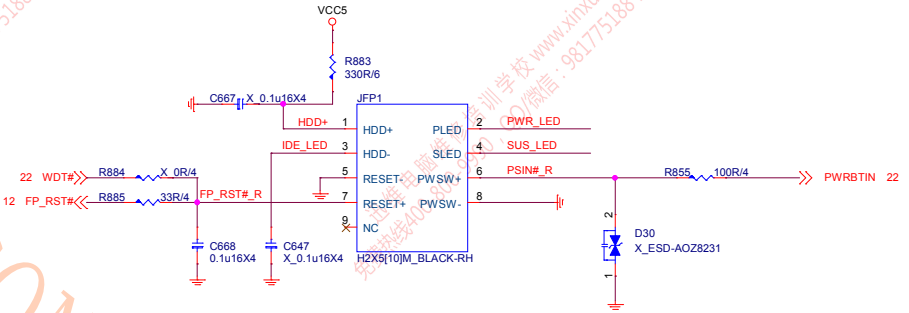
ATX POWER CONNECTOR

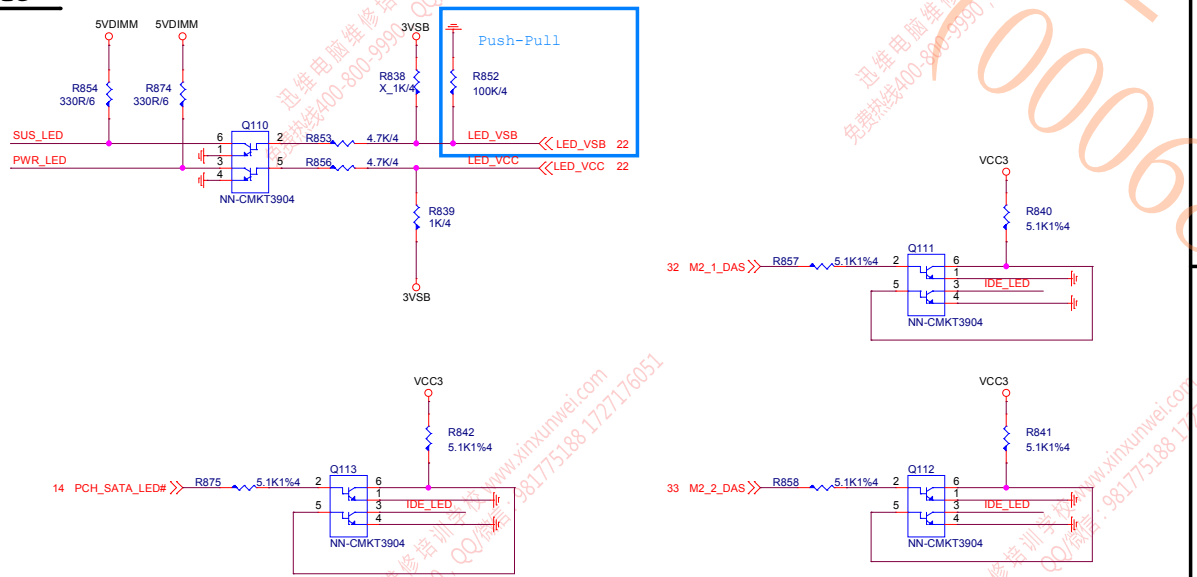
D26:By Ivy's word document.
Main:D0G-1300500-A68
Avl:D0G-3000600-L07/D0G-1200520-I05



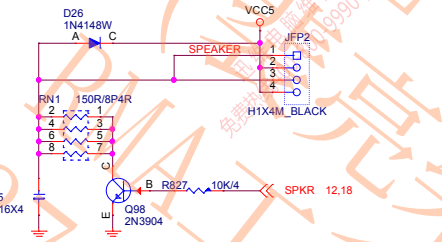
FRONT PANNEL



LED

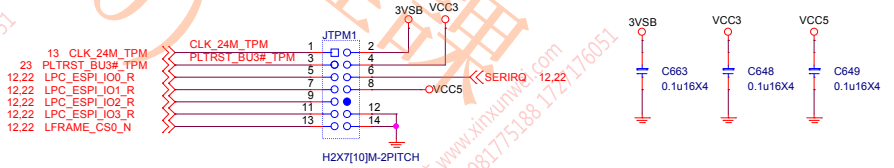


Speaker Pin Header



TPM

Don't colay espi debug.



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MS-7B23		
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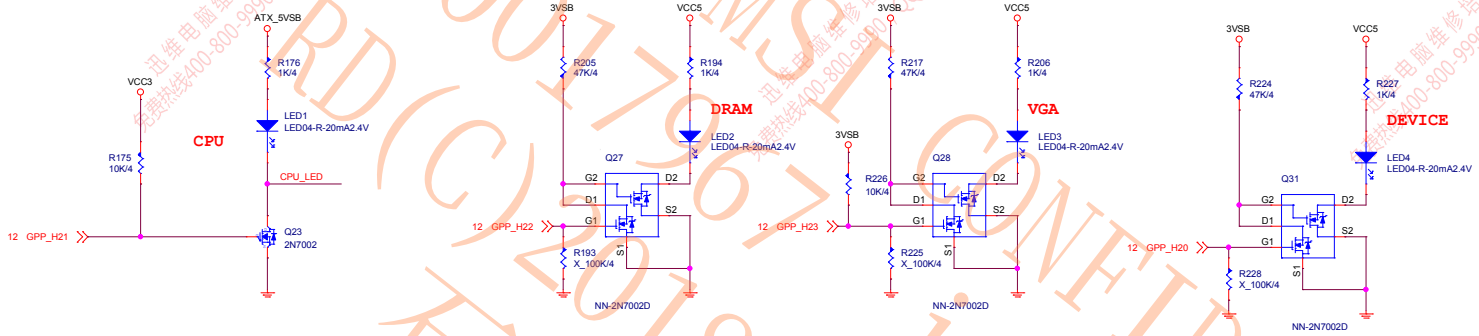
DEBUG LED



RED
PN:D0C-040P100-H91
AVL:D0C-040S500-E07

2018.01.12
PCB2.1 default white LED

WHITE
PN:D0C-040T200-H91
AVL:D0C-040S200-E07

GPIO / LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

開機斷電狀態下，3個LED先維持default全暗，開機通電後：
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

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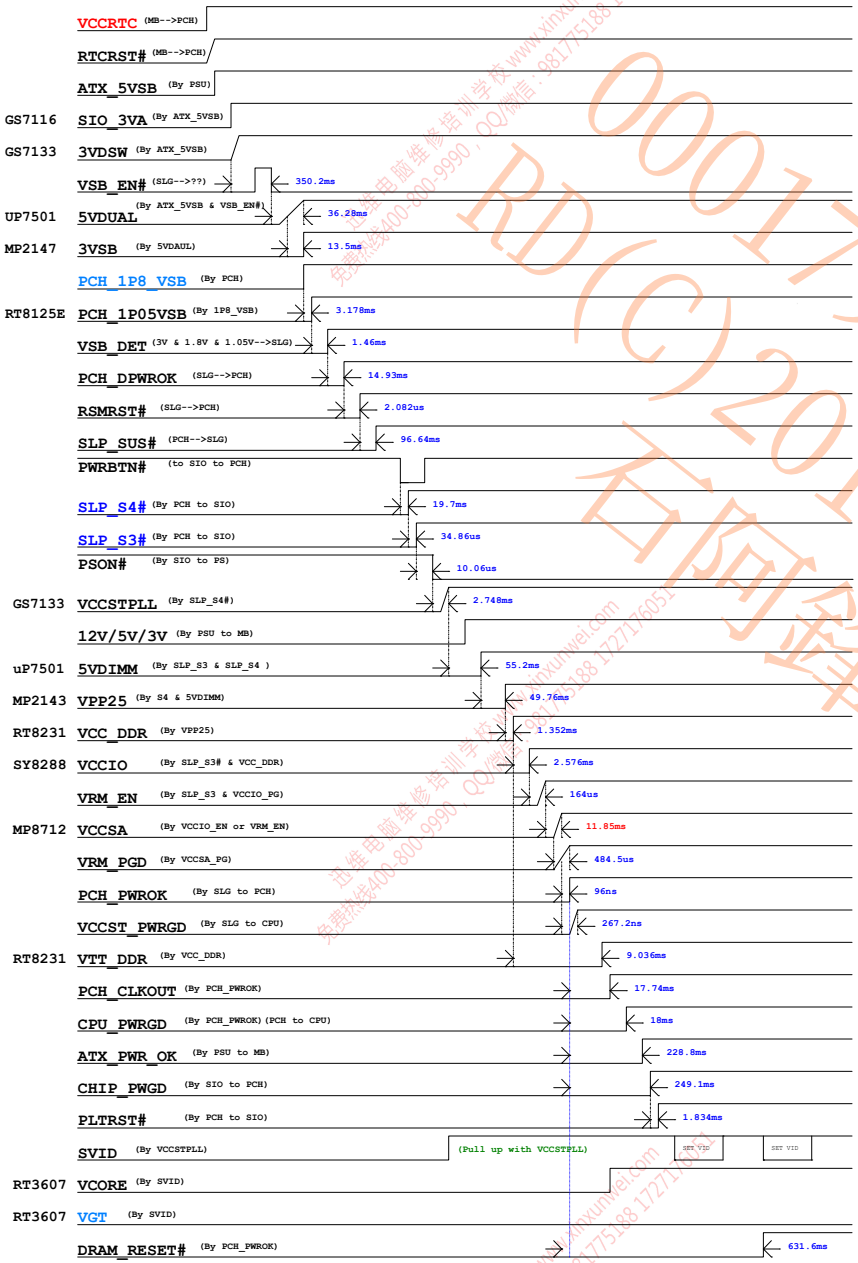
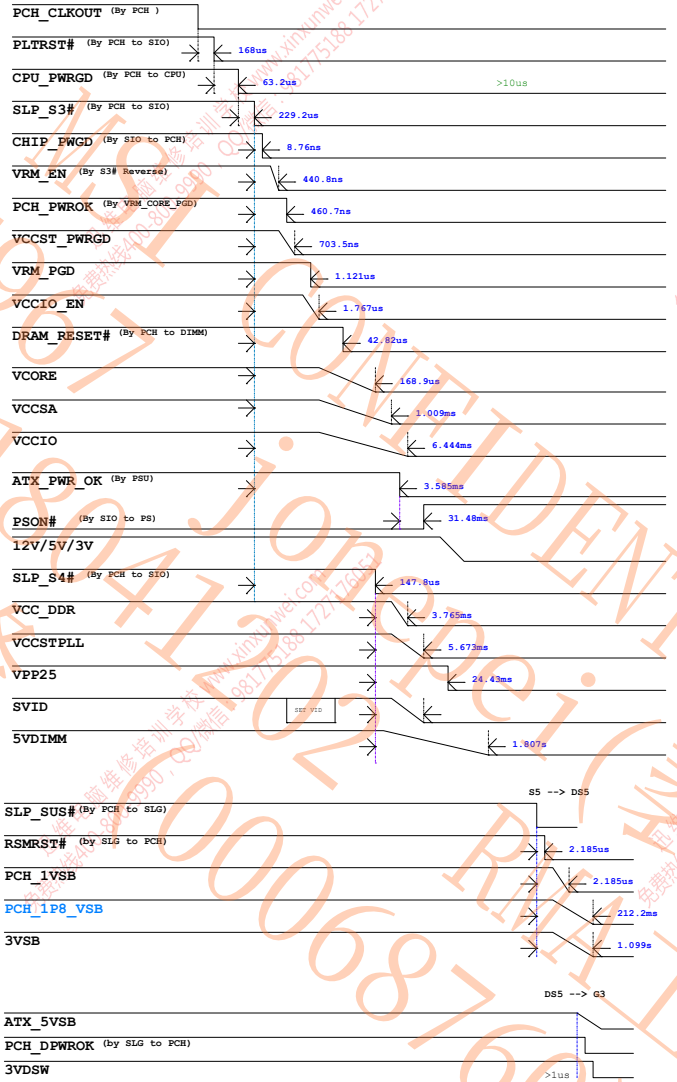
(G3)DS5 ---> S0



S0 ---> DS5(G3)



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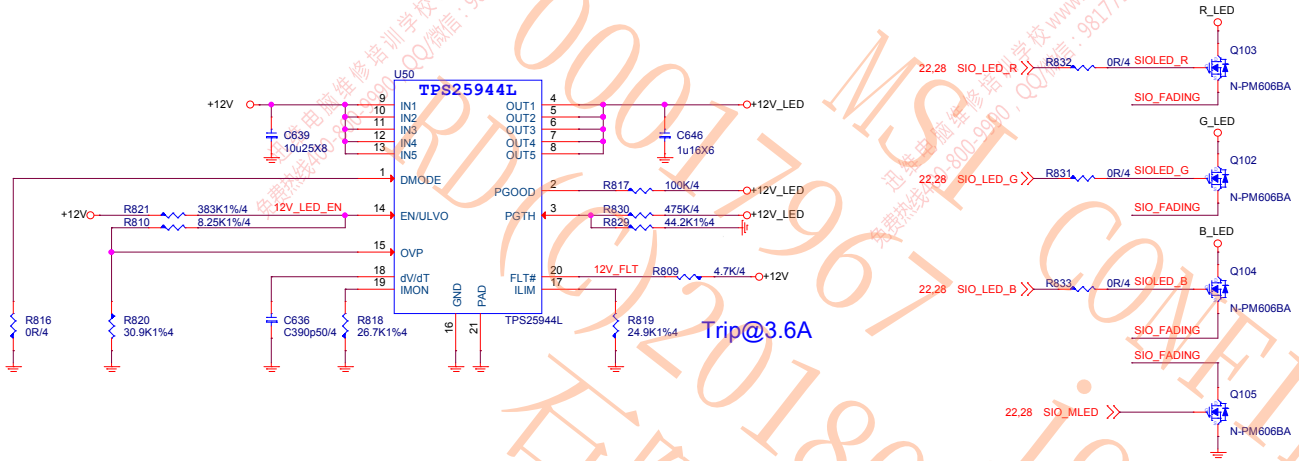
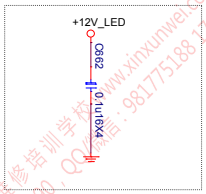
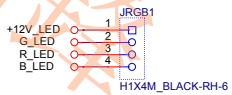
LED STRIPLINE

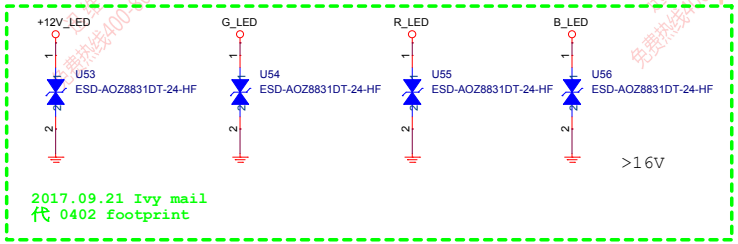


2016.08.02 Add +12V_LED 0.1uF





2016.07.06 only reserve now
2016.08.02 stuff ESD



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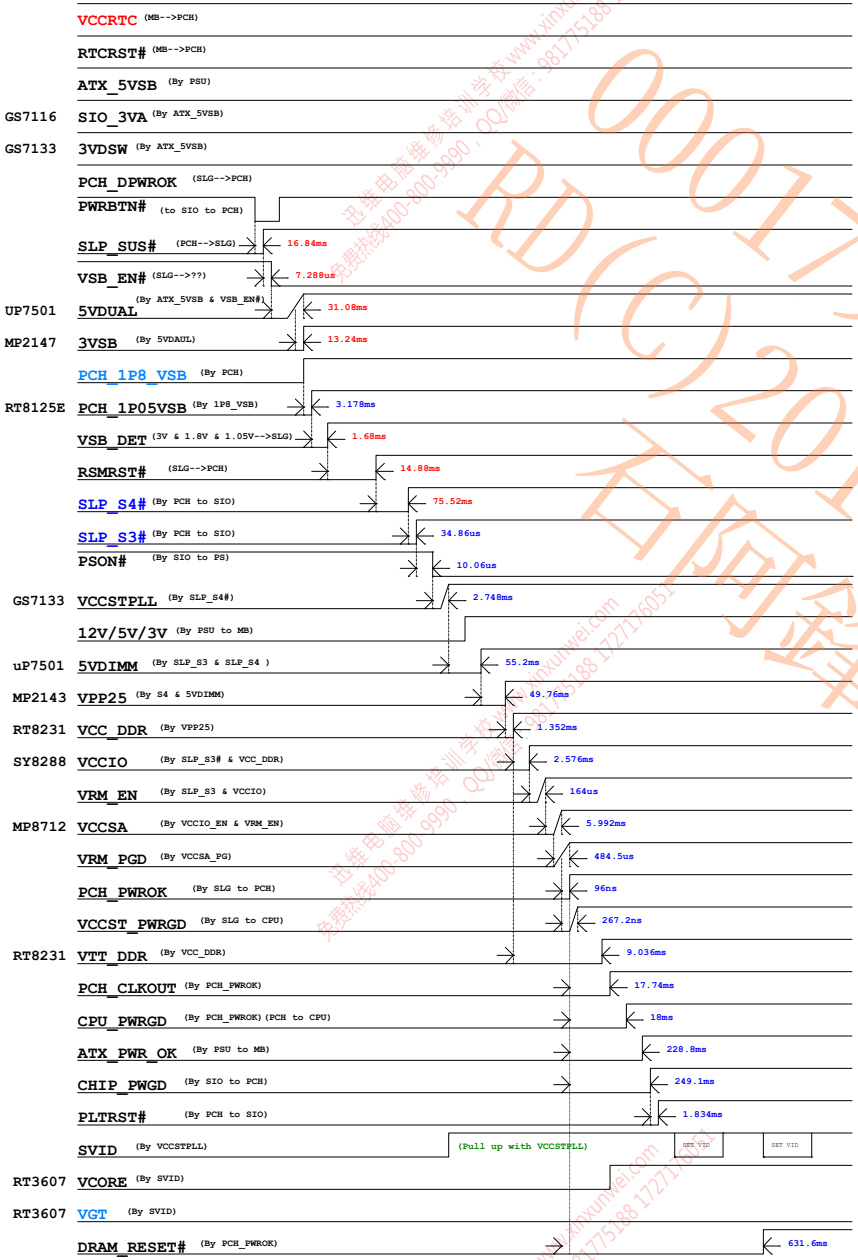
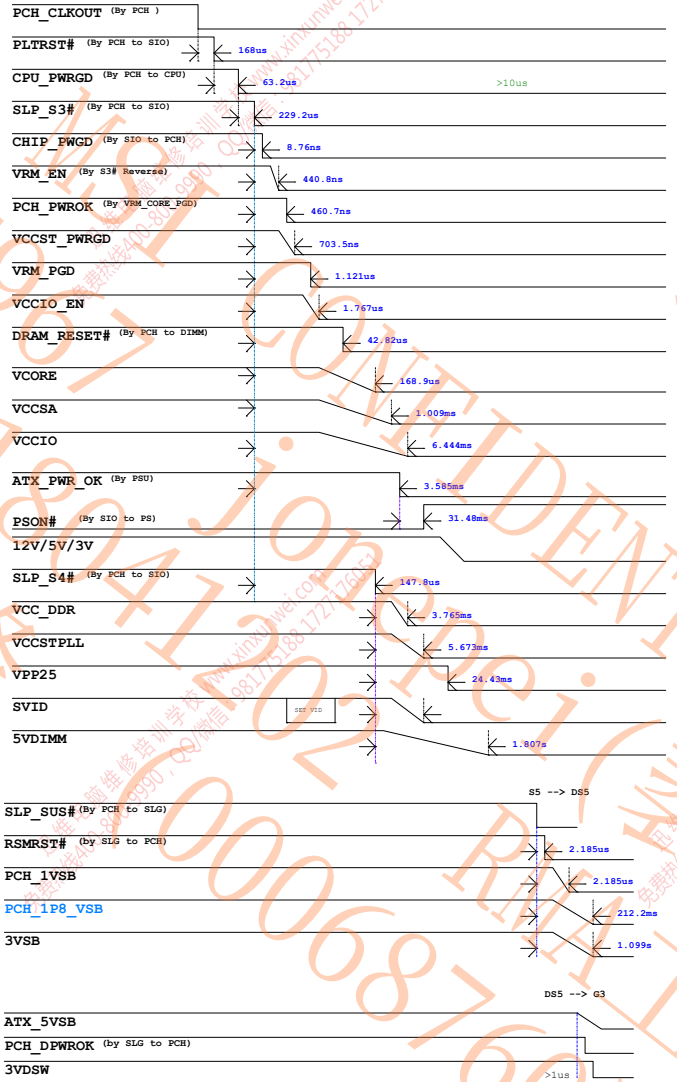
DS5 ---> S0



S0 ---> DS5(G3)



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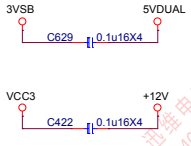
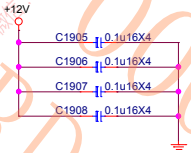
EMI CAP

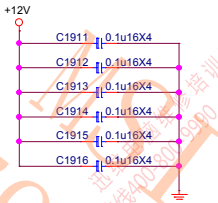
2017.10.13 moat cap



2017.12.21 SA_PH decouple cap



2018.02.02 SA_PH decouple cap



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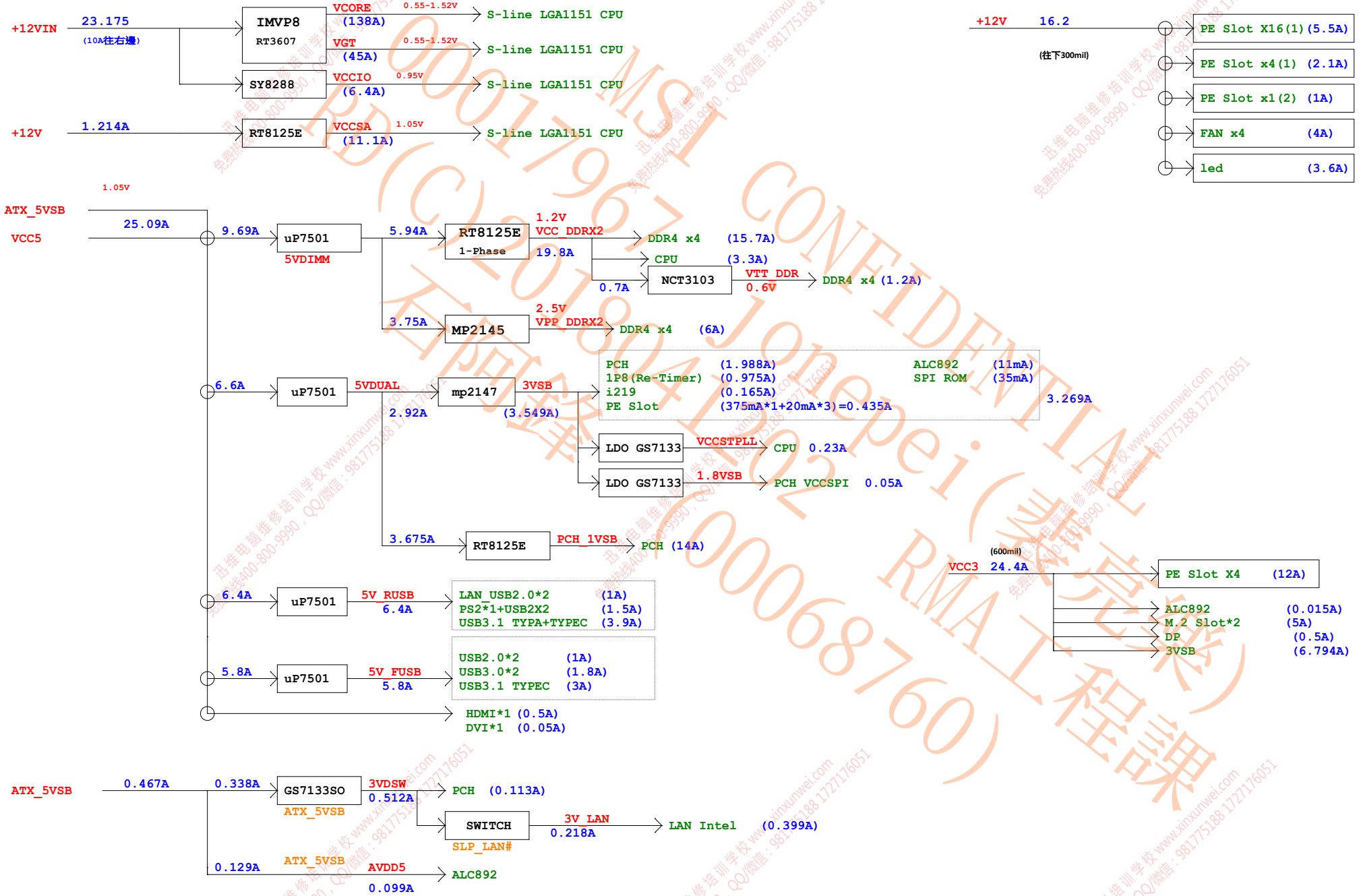
Power Delivery



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RD(C)2018.04.02
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(0000068760)

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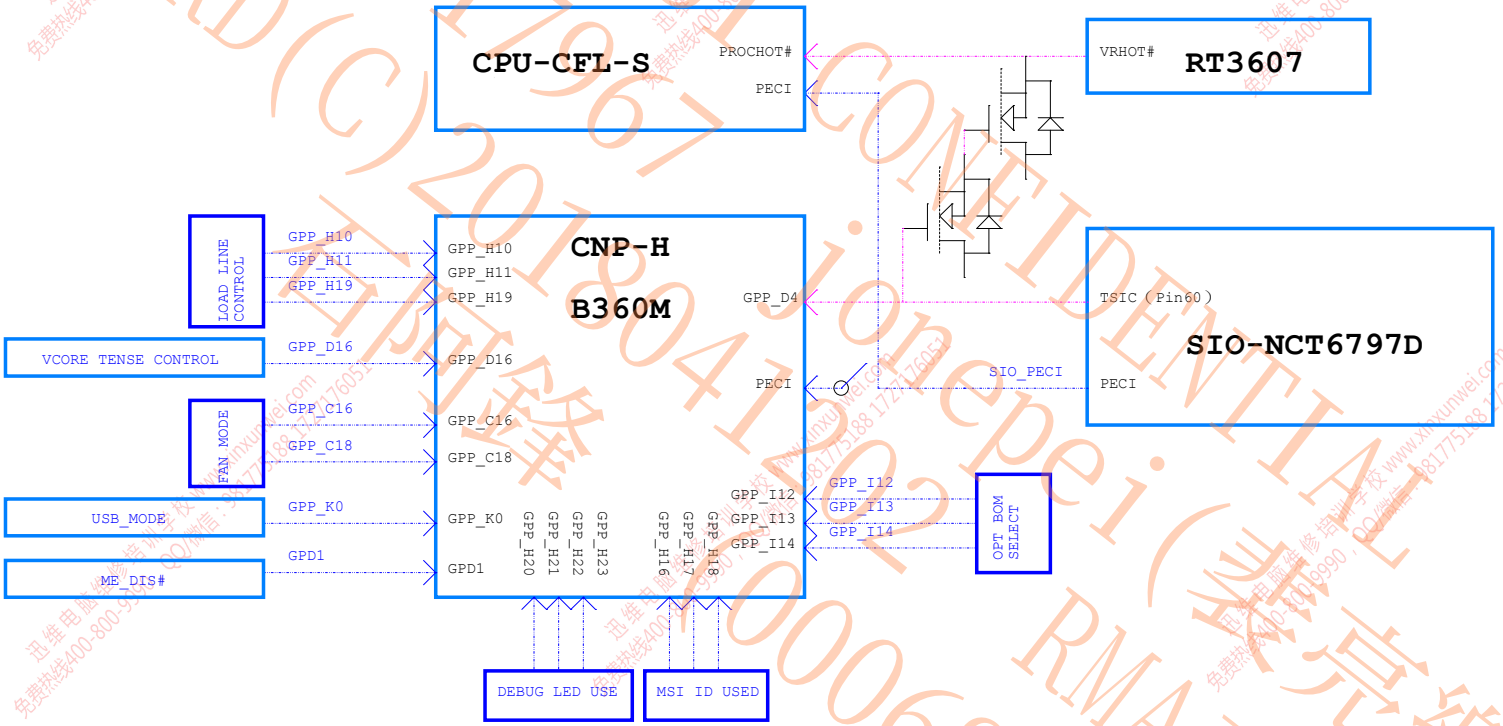

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RD(C)20180412(2)
工程錄 0006876(0)
RMA工程課

0A :

1. 9/14 Jessica mail , add JCOM1 & JTBT1
2. 9/14 Ivy mail , remove PCH_1P05 OV ,change to VCCSA & VCCIO
3. Type-C VCON OC# 線路要改 PU 電壓

1.0 :

1. add SILEGO for power sequence
2. 11/28 M2_1 support to 22110
3. 12/06 TI Re-Driver change to ASM Re-Timer
4. 12/13 remove M.2 screw E43-1203514-A89

2.1 :

1. add SILEGO for power sequence
2. 11/28 M2_1 support to 22110
3. 12/06 TI Re-Driver change to ASM Re-Timer
4. 12/13 remove M.2 screw E43-1203514-A89
5. 12/14 Mortar Arctic -> Mortar Titanium
6. 12/14 CPU_PWR1 change to silver
7. 18/01/12 EZ debug led -> white

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